CS MANTECH™

2009
International Conference on Compound Semiconductor Manufacturing Technology

May 18th – 21st 2009

Register Online at
www.csmantech.org

Tampa Marriott Waterside
Hotel and Marina
Tampa, Florida, U.S.A.

CONFERENCE AT A GLANCE

SUNDAY, May 17th

6:30 PM – 8:30 PM	REGISTRATION Office 1 & 2

MONDAY, May 18th

7:00 AM – 9.00 PM	REGISTRATION Office 1 & 2
7:30 AM – 8:45 AM	Buffet Breakfast Florida Salon 5-6
8:45 AM – 5:00 PM	**WORKSHOPS** Florida Salon 5-6
11:45 AM – 12:45 PM	**WORKSHOP LUNCHEON** Florida Salon 5-6
6:00 PM – 9:00 PM	**EXHIBITS RECEPTION** Grand Ballroom

TUESDAY, May 19th

7:00 AM – 6:00 PM	REGISTRATION Office 1 & 2
7:00 AM – 8:30 AM	Continental Breakfast Grand Ballroom (Exhibits hall)
7:00 AM – 6:00 PM	Internet Café Gallery
8:00 AM – 8:30 AM	**OPENING CEREMONIES** Florida Ballroom
8:30 AM – 10:00 AM	**SESSION 1: Plenary I** Florida Ballroom
10:00 AM – 5:30 PM	**EXHIBITS OPEN** Grand Ballroom
10:00 AM – 10:30 AM	BREAK Grand Ballroom
10:30 AM – 12:00 PM	**SESSION 2: Plenary II** Florida Ballroom
12:00 PM – 1:30 PM	**EXHIBITS LUNCH** Grand Ballroom
1:30 PM – 3:20 PM	**SESSION 3** Florida Salon 1-4
1:30 PM – 3:10 PM	**SESSION 4** Florida Salon 5-6
3:10 PM – 3:40 PM	BREAK Grand Ballroom
3:40 PM – 5:30 PM	**EXHIBITOR'S FORUM 1 - 3** Meeting Rooms 1,4,7
3:40 PM – 5:30 PM	**STUDENT FORUM** Florida Salon 5-6
6:30 PM – 10:30 PM	**INTERNATIONAL RECEPTION** Jackson's Bistro 601 S.Harbour Island Blvd

WEDNESDAY, May 20th

7:00 AM – 5:00 PM	REGISTRATION Office 1 & 2

7:00 AM – 9:30 AM	Continental Breakfast Grand Ballroom (Exhibits hall)
7:00 AM – 7:00 PM	Internet Café Gallery
7:00 AM – 12:00 PM	**EXHIBITS OPEN** Grand Ballroom
9:00 AM – 10:40 AM	**SESSION 5** Florida Salons 1-4
9:00 AM – 10:40 AM	**SESSION 6** Florida Salons 5-6
10:40 AM – 1:00 PM	LUNCH BREAK Open
1:00 PM – 2:40 PM	**SESSION 7** Florida Salons 1-4
1:00 PM – 2:40 PM	**SESSION 8** Florida Salons 5-6
2:40 PM – 3:00 PM	BREAK Florida Foyer
3:00 PM – 4:20 PM	**SESSION 9** Florida Salons 1-4
3:00 PM – 4:50 PM	**SESSION 10** Florida Salons 5-6
5:30 PM – 7:00 PM	**RUMP SESSION RECEPTION** Florida Foyer
6:00 PM – 7:00 PM	**RUMP SESSIONS A-D** Meeting Rooms 1, 2, 3, and 4
7:00 PM – 9:00 PM	**SEMI Standards Meeting** Meeting Room 7
7;30 PM- 11:30 PM	**CHAIRMAN'S EVENING**. SideBern's 2298 W. Morrison Ave.

THURSDAY, May 21st

7:00 AM – 9:30 AM	REGISTRATION Office 1 & 2
7:00 AM – 8:30 AM	Continental Breakfast Florida Foyer
7:00 AM – 4:00 PM	Internet Café Gallery
8:00 AM – 9:20 AM	**SESSION 11** Florida Salons 1-4
9:20 AM – 9:40 AM	BREAK Florida Foyer
9:40 AM – 11:40 AM	**SESSION 12** Florida Salons 1-4
11:40 AM – 1:00 PM	LUNCH BREAK Open
1:00 PM – 2:20 PM	**SESSION 13** Florida Salons 1-4
1:00 PM – 2:30 PM	**SESSION 14** Florida Salons 5-6
2:30 PM – 4:00 PM	**INTERACTIVE FORUM** Grand Ballroom
4:00 PM - 4:30 PM	**CLOSING RECEPTION** Grand Ballroom

MESSAGE FROM THE CONFERENCE CHAIR

In this turbulent year, we are all being swept along in a tsunami of economic change. Manufacturers must adapt to unpredictable markets, inventory corrections, and tighter access to capital. The compound semiconductor industry is well positioned to weather this storm. As a source of technological change, we enable doing more with less. As a driver of creative destruction, the compound semiconductor industry will emerge from economic upheaval both leaner and broader.

Join us in Tampa to discuss the future of compound semiconductor manufacturing. The conference will open with a presentation on how tighter capital markets will impact our industry. Throughout the week, speakers will discuss technologies that will broaden our industry. We will hear about new applications, some in early stages of development, others beginning commercial deployment. The special session on photovoltaic technologies is just one example of how compound semiconductors will boldly go where older technologies have gone before.

This is the annual event where our industry comes together. CS MANTECH's mission is to foster communication between participants from academia, industry, and government. There will be a broad array of educational opportunities including our Monday workshops. Students can interact with potential employers. Industry veterans can keep contact with old friends, meet new ones, and take the pulse of the industry.

The days will be full and so will the nights. The Monday night Exhibits Reception is simply the industry's best networking opportunity of the year. On Tuesday night at Jackson's Bistro, we will have hot music and cold beverages with a waterfront view. It's Florida! On Wednesday night, we will enjoy the Chairman's Evening at SideBurns, one of Tampa's best restaurants.

This is an unusual year. But as usual, this conference is THE event to attend if you want to know what is going on. When visibility is limited by a foggy economy, radar becomes a more critical tool. In Tampa you can check the business radar, keep up with technical developments, and have a great time with those who know the industry best. Bring your boss! She needs to see things first hand too.

Scott Davis
Sumitomo Electric Industries
Chairman, 2009 CS MANTECH Conference

2009 CONFERENCE SPONSORS
(Partial list, as of Feb 14th , 2009)

MANTECH is an independent not-for-profit organization whose mission is to promote technical discussion and scientific education in the compound semiconductor manufacturing industry. The continued success of the conference is enabled by donations from corporate sponsors. The 2009 CS MANTECH Conference Committee gratefully acknowledges the support from our sponsors.

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2009 CONFERENCE HIGHLIGHTS

The 2009 CS MANTECH program begins on Monday May 18th with a series of tutorial workshops. This year's workshops will focus on manufacturing and reliability. This is a must for all technologists who want their devices to operate well into the future.

Monday evening the Exhibits open at 6:00 pm with the traditional Exhibits Reception. The CS MANTECH exhibits are an excellent opportunity to view suppliers of materials, services and tools from around the globe. This is a great time to renew your old relationships and establish new ones while enjoying the fare and libation of Tampa.

The Conference formally opens Tuesday morning. After a brief overview, the awards for the best papers from the 2008 conference will be presented followed by the Plenary Session. Topics in the Plenary Session will cover the breadth of our industry, and will include the current economic downturn, the latest from the DARPA wide band-gap program, CPV solar cell technology, CS devices for automobiles, GaN for base stations and the essentials of running a pure GaAs foundry

After lunch in the Exhibits Hall, Tuesday afternoon will start our parallel sessions of world class technical and business insight of the compound semiconductor industry. Tuesdays technical sessions will conclude with our Exhibitor's Forum. Also in parallel will be our Student Forum designed to be an interactive session between students and the industry destined to hire them. As Tuesday evening approaches, we will move out of the Marriott, to Jackson's Bistro on Harbour Island where we will eat, drink, enjoy live music and a waterfront view.

Wednesday and Thursday continue the stream of excellent technical papers on compound semiconductor manufacturing technology. The late start allows for additional opportunity to interact in with the Exhibitors before the Exhibits close at noon. One side of Wednesday's parallel sessions focuses on emerging wide band-gap technologies, while the other covers process, yield, device reliability and wafer fab management. These are topics for which CS MANTECH is well known.

Wednesday evening features the popular Rump Sessions. Eat, drink, and debate! Attendees may join any or all (if you move quickly) of the four parallel topics, where moderators will encourage informal, lively and highly interactive discussions. Following the Rump Session will be the Chairman's Evening, located at SideBurns, one of Tampa's best restaurants. Open bar!

Thursday morning continues the excellent technical papers on devices, processing, circuits, and manufacturing. Thursday afternoon holds our closing two sessions and our Interactive Forum poster session. The poster session includes papers on a diverse range of topics, as well as posters of all the papers presented earlier in the technical program. Attendees will have an excellent opportunity to meet with authors to discuss their papers. During the Forum, attendees will vote for the best poster and the winning author will receive the Best Poster Award.

The Conference Closing Reception will follow the Interactive Forum. In a warped tilt to our historic "Ugly Picture Contest" we will holding an "Ugliest Process Tool Contest". Our closing reception will also feature a drawing for an iPod Touch. All those who completed and submitted their Feedback Forms will have a chance to win!

WORKSHOPS

Each year in conjunction with the technical program, CS MANTECH offers Monday workshops on topics of interest to the compound semiconductor community. Past programs have offered tutorials on areas ranging from materials and processing, test and characterization, applications and market analysis, to engineering management and intellectual property rights. These invited talks by industry and academic leaders offer a forum for in-depth presentations and instruction.

This year's theme is **Manufacturing and Reliability**. Significant advances in manufacturing processes and device/circuit performance have been, and are being, made by the compound semiconductor community. However, if the technology is unreliable, it will never be used. Reliability and the underlying manufacturing processes are critical areas to be understood. To this end, CS MANTECH is pleased to offer a day of talks on this subject that will focus on the reliability assessment process and robust manufacturing analysis. The planned tutorials will provide a good overview for those just wanting to learn more, but will provide sufficient breadth of topics and detail that even those in the field will learn something new.

The morning will begin with a talk titled "Moving from Reliability to Manufacturability" given by Mr. Bill Roesch from TriQuint Semiconductor. Mr. Roesch is a dynamic speaker and a conference favorite having won a number of "Best Paper" awards. He is an expert in the field of compound semiconductor reliability and brings decades of experience, data and analysis to the task of understanding

the connection between robust manufacturing processes, yield and reliability. In addition to a historical perspective of CS reliability and a discussion on the conventional reliability assessment process, Mr. Roesch will present new material showing how device/circuit lifetime is linked to a robust manufacturing process. After a short break, Mr. Kevin Berger from Analytical Solutions, Inc will discuss an array of techniques that can be used in root cause investigations in his talk "Failure Analysis – Fault Localization." An activation energy and extrapolated lifetime are useful (and often necessary) figures of merit for semiconductor technology, but ultimately we need to understand the degradation mechanism causing the part to fail. Techniques discussed will include non-invasive microscopy (optical, x-ray and acoustic), electrical isolation (photoemission and liquid crystal), and electron beam analysis such as scanning electron beam (SEM) imaging, electron beam induced current (EBIC) imaging, and voltage contrast (VC) imaging.

The afternoon sessions will begin with a talk by Dr. Mike Salmon of Evans Analytical Group titled "Transmission Electron Microscopy (TEM) Based Failure Analysis." Fault sites localized via techniques described in the morning session can be examined at the atomic level through TEM analysis. The EAG talk will describe site specific cross-sectional TEM characterization. Topics will include sample preparation techniques, S/TEM imaging, and chemical analysis. Examples of TEM based failure analysis will be discussed. Professor Jesus del Alamo of Massachusetts Institute of Technology (MIT) will follow with a discussion on step stress analysis in his talk titled, "Electrical, Thermal and Environmental Reliability of Transistors: Experimental Techniques to Identify Fundamental Degradation Mechanisms." Professor del Alamo will contrast step stress analysis with the traditional three temperature accelerated life test procedure routinely performed in conventional reliability assessments. Examples of how alternative stressors can be applied in step stress analysis will be described along with results from the process.

The last session of the day begins with the talk "Fully Coupled Process and Device Simulation for Understanding Reliability" from Professor Mark Law from the University of Florida. Professor Law will describe how process simulation can be used to help understand degradation phenomenon. For example, how can modeled defect behavior help predict dopant diffusion and activation? Methodology for simulating these effects and initial results from a case study will be presented. The final presentation is from Professor Martin Kuball from the University of Bristol titled, "Modern Thermography for Semiconductor

Technology for Reliability Testing: Channel Temperature and Stresses/Strains in Devices." Lifetime projections are predicated on accurate channel temperature estimates. Professor Kuball will provide an overview of techniques used to measure channel temperature with an emphasis on micro Raman analysis.

INDUSTRY EXHIBITS

CS MANTECH's exhibits provide an opportunity for device manufacturers to see suppliers of equipment, materials, and other services in a single location. Industry suppliers have long known that CS MANTECH's exhibition is *the* opportunity of the year to congregate with the key players in the compound semiconductor field.

Monday evening's Exhibits Reception is simply the best networking opportunity in our industry. Everyone is there, food is provided, the bar is open, and no one has to drive home. Tuesday will begin with a continental breakfast in the Exhibits Hall at 7.00 am. Following the Plenary Session, the Exhibits will open and be the location for the extended coffee breaks and our buffet style Exhibits Lunch (12.00 pm -1:30 pm). Attendees have ample opportunity to greet old friends and meet new ones. The exhibits will stay open on Wednesday from 7.00 am until 12.00 pm. This additional half-day is scheduled to allow for discussion with Exhibitors following presentations at the Tuesday afternoon Exhibitor's forum (see below).

Those who know reserve their booth space early. The exhibits often sell out, so you would be wise to book your space now. Visit our web site at www.csmantech.org, and click on the Exhibitors link. For any questions please contact Mike Barsky, Exhibits Chair, 310-814-1946
email: exhibitor@gaasmantech.org

EXHIBITORS FORUMS

The exhibitor's forums allow participating companies to introduce new products or highlight company strengths in a short presentation. This year's forums will be on Tuesday from 3:40 pm – 5:30 pm. With the extended exhibit hours on Wednesday, attendees and exhibitors will have the opportunity for discussion after the forum presentations. Presentation slots can be requested when signing up for a booth on the web site. Presentation slots are limited, so sign up early!

INTERNATIONAL RECEPTION

This year's International Reception will be held at Jackson's Bistro, one of Tampa's premier restaurants and nightclubs. Specializing in sushi, seafood, and Asian Fusion cuisine, Jackson's is only a short stroll across the bridge from the conference hotel. We will be able to watch the sunset over Tampa Bay while dining on exquisite food, and enjoying cocktails, beer and wine. A local band will be providing live music for dancing (especially after several of the aforementioned cocktails….). So practice your samba and salsa dancing, and come prepared to enjoy a spectacular evening. Guest tickets are $50 each and available at the Registration Desk. *We strongly encourage you to purchase guest tickets at the time of your registration to ensure space at the reception.*

2008 BEST PAPER AWARDS

CS MANTECH tradition is to formally recognize the authors of the best paper and best student paper of the previous conference, as determined from the conference attendee votes tallied from *your* feedback forms. These awards will be presented during the conference introductions on Tuesday, May 19th.

The conference Best Paper Award is named in honor of Dr. He Bong Kim, the founder of the International Conference on Compound Semiconductor MANufacturing TECHnology. The He Bong Kim award winners for the 2008 Conference are Dorothy June, M. Hamada and William J. Roesch for their paper on *"Reliability and MMIC Technology Development and Production"*

The Best Student Paper voting for the 2008 Conference resulted in a co-award:, William Snodgrass and Milton Feng, University of Illinois for *"Nano-scale Type-II InP/GaAsSb DHBTs to reach THz Cutoff Frequencies"* and David J. Meyer, Joseph R. Flemish and Joan M. Redwing, Pennsylvania State University for *"Pre-passivation Plasma Surface Treatment Effects on Critical Device Electrical Parameters of AlGaN/ GaN HEMTs"*

The principal student authors, William Snodgrass and David J. Meyer respectively, will each receive a special cash award of $1000.

Congratulations to these award winning teams for their fine work!

SEMI STANDARDS MEETING

The SEMI Standards meeting is scheduled for Wednesday, May 20th, from 7:00 pm to 9:00 pm (immediately following the Rump Sessions) in Meeting Room 7. The SEMI Compound Semiconductor (GaAs, InP and SiC) Committee invites CS MANTECH Conference attendees interested in the development of internationally approved standards for wafer specifications to attend this meeting. Topics being addressed are GaAs, InP, and SiC dimensions/orientations and electrical properties, epitaxial layer specifications (which properties should be specified, and how they are to be verified), and non-destructive test methods.

Based in San Jose, CA, SEMI is an international trade association serving more than 2,400 companies participating in the semiconductor and flat panel display equipment and materials markets. SEMI maintains offices in Brussels, Moscow, Tokyo, Seoul, Hsinchu, Beijing, Singapore, Austin, Boston and Washington, DC. For additional information, please contact: Co-Chair: James Oliver of Northrop Grumman at 410-765-0117 or *j.oliver@ngc.com*, Co-Chair: Russ Kremer of Freiberger Compound Materials at 937-291-2899 or *russ@fcm-us.com*, or SEMI Standards Engineer Ian McLeod at 408-943-6996 or *imcleod@semi.org*.

UGLIEST PROCESS TOOL COMPETITION

What old equipment is YOUR fab still using? We're having another of the MANTECH infamous photo contests and are seeking the oldest manufacturing equipment still being used in production!

We're soliciting photo entries of wafer manufacturing **equipment that is used on a routine basis, as part of the regular manufacturing scheme**. Sorry, but if it's sitting in a warehouse, it's ineligible. What do YOU have that qualifies?

Please submit a photo showing your **antiquated equipment**, along with appropriate identification (make, model, year, etc). A prize will be awarded based on attendee voting during the Interactive Forum. Your vendor will LOVE this. Your Equipment Maintenance guys will be proud. And if you're really lucky, your boss will be SO embarrassed he'll fund a new acquisition to replace that piece of junk!! Contact Jim Crites for more information: james.crites@cobhamdes.com

CONFERENCE CLOSING RECEPTION

The Conference Closing Reception will bring to an end the 2009 edition of CS MANTECH. It will immediately follow the Interactive Forum. Drinks and snacks will be provided to foster a congenial final opportunity to exchange business cards, ideas, and experiences.

Returning this year is a Feedback Form Raffle. Your opinion on the Feedback Form is very valuable to the CS MANTECH committees in structuring the conference and programs year-to-year and in choosing the best paper awards. This year, when you turn in your Feedback Form you enter a raffle for an iPod Touch. It's as simple as that. The drawing will be held at the Conference Closing Reception, though you need not be present to win. In addition, votes will be tallied and the Best Poster presentation and Ugliest Process Tool Award winners will be announced.

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TECHNICAL PROGRAM
Monday, May 18th

WORKSHOPS

Chair: David Via, *Air Force Research Laboratory*

Workshop Session 1
8;45 AM **Moving from Reliability to Manufacturability**
Bill Roesch , TriQuint Semiconductor

10:30 AM BREAK

Workshop Session 2
10:45 AM **Failure Analysis – Fault Localization**
Kevin Berger, Analytical Solutions, Inc.

11;45 AM **WORKSHOP LUNCHEON**

Workshop Session 3
12:45 PM **Transmission Electron Microscopy (TEM) Based Failure Analysis**
Mike Salmon,, Evans Analytical Group

Workshop Session 4
12:45 PM **Electrical, Thermal and Environmental Reliability of Transistors: Experimental Techniques to Identify Fundamental Degradation Mechanisms.**
Jesus del Alamo, MIT

2:45 PM **BREAK**

Workshop Session 5
3:00 PM **Fully Coupled Process and Device Simulation for Understanding Reliability**
Mark Law, University of Florida.

Workshop Session 6
3:00 PM **Modern Thermography for Semiconductor Technology for Reliability Testing: Channel Temperature and Stresses/Strains in Devices**
Martin Kuball, University of Bristol

6:00 PM **EXHIBITS RECEPTION**

Tuesday, May19th

8:00 AM **Conference Opening**
Scott Davis, Sumitomo Electric
Conference Chair

8:10 AM **2008 Conference Best Paper Awards**
Steve Mahon TriQuint Semiconductor
Technical Program Chair

8:20 AM **Technical Program Highlights**
Steve Mahon TriQuint Semiconductor
Technical Program Chair

SESSION 1: PLENARY I

Chair: Steve Mahon, *TriQuint Semiconductor*

8:30 AM *Invited Presentation*
1.1 The Impact of the Current Financial Crisis on the Compound Semiconductor Industry
Earl Lum, EJL Wireless Research LLC

9:00 AM *Invited Presentation*
1.2 The DARPA Wide Band Gap Semiconductor for RF Applications (WBGS-RF) Program: Phase II Results
M. Rosker[1], C. Bozada[2], H. Dietrich[3], A. Hung[4], S. Binari[5], G.D. Via[2], E. Viveiros[4], E. Cohen[6], and J. Hodiak[7],
[1]DARPA, [2]AFRL, [3]ONR, [4]ARL, [5]NRL
[6]EBCO, [7]BAH

9:30 AM *Invited Presentation*
1.3 Opportunities for Development of a Mature Concentrating Photovoltaic Power Industry
Sarah Kurtz, National Renewable Energy Laboratory

10:00 AM **BREAK**

SESSION 2: PLENARY II

Chair: Steve Mahon, *TriQuint Semiconductor*

10:30 AM *Invited Presentation*
2.1 Wide Bandgap Devices for Automobiles
Tetsu Kachi Toyota

11:00 AM *Invited Presentation*
2.2 GaN for Base Stations
Bill Vassilakis, Powerwave

11:30 AM *Invited Presentation*
2.3 A Successful Pure Foundry Business
C.C. Chang, WIN Semiconductor

12:00 PM **EXHIBITS LUNCH**

SESSION 3: SOLAR CELLS

Chair: Noran Pan, *MicroLink Devices*

1:30 PM *Invited Presentation*
3.1 CdTe Based Solar Technology
Walt Wohlmuth, First Solar Inc.

2:00 PM *Invited Presentation*
3.2 Concentrating Solar Energy-Technologies and Markets Overview
Raed Sherif, eSolar Inc.

2:30 PM **3.3 Triple-Junction Solar Cells (TJ-SC) – Support from MOCVD for Competitiveness through Improved Material Quality and Cost Reduction**
B. Schineller, J. Hofeldt, R. Schreiner, G. Strauch and M. Heuken, AIXTRON AG

2:50 PM *Invited Presentation*
3.4 Status of Multijunction Solar Cells and Future Development
Tatsuya Takamoto, SHARP Corp.

3:20 PM **BREAK**

SESSION 4: RELIABILITY/TEST

Chair: Paul Werbaneth, *Tegal Corp.*

1:30 PM *Invited Presentation*
4.1 High Frequency Wafer Level Reliability Test Bench with Variable Load Impedance
P. Abele, F. Bourgeois, M. Lanz, J. Grünenpütt, R. Behtash, J. Thorpe and D. Behammer, United Monolithic Semiconductors

2.00 PM *Student Presentation*
4.2 Lifetime Estimation of Intrinsic Silicon Nitride MIM Capacitors in a GaN MMIC Process
Sefa Demirtas[1], Jesus A. del Alamo[1], Donald A. Gajewski[2] and Allen Hanson[2]
[1]Massachusetts Institute of Technology, [2]Nitronex Corporation

2:20PM **4.3 PECVD Silicon Nitride Film Property and Pre-deposition Surface Treatment Effects on MIMCAP Reliability for InGaP/GaAs HBT Applications**
Tong Wang, Anadigics, Inc.

2:40PM **4.4 Investigating the ESD Robustness of RF Circuits and Elements by Transmission Line Pulsing**
Heinrich Wolf, Horst Gieser and Karlheinz Bock, Fraunhofer-Institute

3.00 PM **4.5 RF Test Gage R&R Improvement**
James Oerth and Mike Downs, Skyworks Solutions Inc.

3:20 PM **BREAK**

3:40 PM: **EXHIBITORS FORUMS**

Please refer to the posted placards in the exhibit area for forum participants and scheduled presentations.

3:40 PM: **STUDENT FORUM**

6:30 PM: **INTERNATIONAL RECEPTION**

Wednesday May 20th

SESSION 5: GaN DEVICES

Chairs: Andy Souzis, *II-VI Corp*. & Robert Sadler, *Nitronex Corp.*

9:00 AM **5.1 Influence of SiC Substrate Misorientation on AlGaN/GaN HEMTs Performance**
K. Matsushita[1], H. Sakurai[1], J. Shim[1], K. Takagi[1] H. Kawasaki[1], Y. Takada[2] and K. Tsuda[2] [1]Microwave Solid-state Department Toshiba Corp. [2]Advanced Electron Devices Laboratory, Research and Development Center, Toshiba Corp.

9:20 AM **5.2 Process Benchmarking of SiC Backside Via Manufacturing for GaN HEMT technology**
H. Stieglauer, B. Klein, G. Bödege, and D. Behammer, United Monolithic Semiconductors

9:40 AM **5.3 Very Low Sheet Resistance AlN/GaN High Electron Mobility Transistors**
C.Y. Chang[1], T.J. Anderson[1], F. Ren[2], S.J. Pearton[1], Amir Dabiran[2], and P.P. Chow[3] [1]Department of Materials Science Engineering, University of Florida, [2]Department of Chemical Engineering, University of Florida [3] SVT Associates

10:00 AM *Student Presentation*
5.4 GaN Field Effect Transistor based Biosensor
Siddharth Alur[1], Hui Xu[1], Yaqi Wang[1], Tony Gnanaprakasa[2], Aleksandr L. Simonian[2],and Minseo Park[1]
[1]Department of Physics, Auburn University, [2]Materials Research and Education Center, Department of Mechanical Engineering, Auburn University.

10:20 AM *Student Presentation*
5.5 Wide Bandgap GaN Smart Power Chip Technology
King-Yuen Wong, Wanjun Chen and Kevin J. Chen, Hong Kong University of Science and Technology

10:40 AM **BREAK**

SESSION 6: PROCESS, METALIZATIONS

Chairs**:** Russ Westerman, *Oerlikon* & Thorsten Saeger, *TriQuint Semiconductor*

9:00 AM **6.1 Processing Methods for Ultra-Low Ohmic Contact Resistance in AlN/GaN MOSHEMTs**
K. Chabak[1], D. Langley[1], A. Crespo[1], M. Trejo[1], V. Miller[1], J.K. Gillespie[1], G.D. Via[1], A.M. Dabiran[2], A.M. Wowchak[2], B. Cui[2], and P.P. Chow[2]
[1]Sensors Directorate, Air Force Research Laboratory, Wright-Patterson Air Force Base, [2]SVT Associates, Inc.

9:20 AM *Student Presentation*
6.2 A Cu Metalized Power InGaP/GaAs with Copper Based Ohmic Contact
S. P. Wang, Y. C. Lin, Y. L. Tseng, K. S. Chen, L. H. Chang and E. Y. Chang, Department of Materials Science and Engineering, National Chiao-Tung University.

9:40 AM **6.3 Copper Interconnect on GaAs pHEMT by Evaporation Process**
Kezia Cheng, Skyworks Solutions

10:00 AM **6.4 TIWN Thin Film Resistor Process Control**
J.W.Crites and M.J.Drinkwine, Cobham Roanoke

10:20 AM **6.5 Process Development of GaAs Based RF MEMS**
P. Suryanarayana[1], A.A. Naik[2], Ch.Sridar[1], V.S.N. Murthy[1], J. Ravikiran[1], M.Renju[1], S.D. Sandeep[1] ,A.V. Prasad[1], S.K. Rao[1]., A. Mangatayaru[3], S.K. Koul[4], and R. Muralidharan[1].
[1]GAETEC [2]MMIC Group, [3]RCI, Vignyana Kancha Post, [4]IIT, DELHI

10:40 AM **BREAK**

SESSION 7: PROCESS/ETCH

Chairs: Michelle Bourke, *Surface Technology Systems* & Scott Sheppard, *Cree Inc.*

1:00 PM **7.1 SiC Backside Via-hole Process For GaN HEMT MMICs Using High Etch Rate ICP Etching**
Naoya Okamoto, Toshihiro Ohki, Satoshi Masuda, Masahito Kanamura, Yusuke Inoue, Kozo Makiyama, Kenji Imanishi, Hisao Shigematsu, Toshihide Kikkawa, Kazukiyo Joshin, and Naoki Hara,
Fujitsu Limited and Fujitsu Laboratories Ltd

1:20 PM **7.2 High-Volume 0.25 µm AlGaAs/InGaAs E/D pHEMT Process Utilizing Optical Lithography**
Corey A. Nevers, Andrew T. Ping, Otto Berger and Tim Henderson, TriQuint Semiconductor

1:40 PM **7.3 SiC Substrate Via Etch Process Optimization**
Ju-Ai Ruan, Sam Roadman, Cathy Lee, Cary Sellers, Mike Regan and Chris Youtsey, TriQuint Semiconductor

2:00 PM **7.4 Influence of Dielectric Plasma Etch Source for PHEMT Device Performance**
F.S. Pool, A. Ping, M. Wilson and B. Berggren, TriQuint Semiconductor

2:20 PM *Student Presentation*
7.5 Fabrication Process of MS-to-CPW RF-Via Transition for RF-MEMS Devices Packaging Applications
Li-Han Hsu[1,2], Wei-Cheng Wu[1,2], Edward Yi Chang [1], Herbert Zirath [2], and Chin-Te Wang [1]
[1]Department of Materials Science and Engineering, National Chiao Tung University, [2]Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, University of Technology, Göteborg

2:40 PM **BREAK**

SESSION 8: RELIABILITY, THERMAL ANALYSIS

Chair: Peter Ersland, *Cobham*

1:00 PM **8.1 Accurate Channel Temperature Measurement in AlGaN/GaN HEMT Devices and its Impact on Accelerated Lifetime Predictive Models**
B. Claflina,[1,2], E. R. Hellera,[1,2], B. Winningham[3] and G. D. Via[3]
[1]Materials and Manufacturing Directorate, AFRL/RXPS, Wright-Patterson AFB,
[2]Semiconductor Research Center, Wright State University,
[3]Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB

1:20 PM *Student Presentation*
8.2 Field Dependent Self-Heating Effects in High-Power AlGaN/GaN HEMTs
M. Hosch[1], J. W. Pomeroy[2], A. Sarua[2], M. Kuball[2], H. Jung[3], and H. Schumacher[1]
[1]Ulm University, Institute of Electron Devices and Circuits, [2]H.H. Wills Physics Laboratory, University of Bristol,
[3]United Monolithic Semiconductors

1:40 PM *Student Presentation*
8.3 Determination of Junction Temperature of GaN-based Light Emitting Diodes by Electroluminescence and Micro-Raman Spectroscopy
Yaqi Wang[1], Hui Xu[1], Siddharth Alur[1], An-Jen Cheng[1], Minseo Park[1], Sharukh Sakhawat[2],Arindra N. Guha[2], Okechukwu Akpa[2], Saritha Akavaram[2] and Kalyankumar Das[2]
[1]Department of Physics, Auburn University,
[2]Electrical Engineering Department, Tuskegee University

2:00 PM *Student Presentation*

8.4 Temperature Diagnosis of Bulk GaN-based Schottky Diode by Raman Spectroscopy

Hui Xu[1], Siddharth Alur[1], Yaqi Wang[1], An-Jen Cheng[1], Kilho Kang[1], Claude Ahyi[1], John Williams[1], Minseo Park[1], Chaokang Gu[2], Andrew Hanser[3], Tanya Paskova[3], Edward A. Preble[3], Keith R. Evans[3], and Yi Zhou[4]

[1]Department of Physics, Auburn University,
[2]Department of Chemistry and Biochemistry, Auburn University,
[3]Kyma Technologies Inc.,
[4]Department of Electrical Engineering, University of California

2:20 PM *Student Presentation*

8.5 Thermal and piezoelectric stress in operating AlGaN/GaN HFET devices and effect of the Fe doping in the GaN buffer layer

A. Sarua[1], T. Batten[1], H. Ji[1], M. J. Uren[2], T. Martin[2] and M. Kuball[1],
[1]H.H. Wills Physics Laboratory, University of Bristol, [2]QinetiQ Ltd.

2:40 PM **BREAK**

SESSION 9: GaN GROWTH AND CHARACTERIZATION

Chairs: John Blevins *AFRL/RXPS* & Ruediger Schreiner *Aixtron AG*

3:00 PM **9.1 Bulk Growth of GaN by HVPE**
H.Ashraf[1], G.W.G. Dreumel[1], J.L. Weyher[2] and P.R. Hageman[1]
[1]Applied Material Science, Institute for Molecules and Materials, University Nijmegen,
[2]Institute of High Pressure Physics, Polish Academy of Sciences

3:20 PM **9.2 Orientation Control of Bulk GaN Substrates Grown via Hydride Vapor Phase Epitaxy**
P.R. Daniels, E. Preble, T. Paskova, and D. Hanser, Kyma Technologies Inc.

3:40 PM **9.3 High Thermal Conductivity of Low Dislocation Density GaN**
Haojun Luo[1], Drew Hanser[2], Edward A. Preble[2], Patrick Wellenius[1] and John F Muth[1]
[1]NC State University, Department of Electrical and Computer Engineering,
[2]Kyma Technologies Inc.

4:00 PM **9.4 PVD Growth of AlN Nucleation Layers for GaN-based LED Structures Offers Cheaper, Brighter Alternative**
T. Clites, E.A. Preble, K.R. Evans, T. Paskova and A. D. Hanser,
Kyma Technologies, Inc.

SESSION 10: FAB MANAGEMENT

Chair: Alex Smith, *Brewer Science*

3:00 PM *Invited Presentation*
10.1 Maintaining a Green Fab through the Strategic Use of an Environmental Management System
Ernest Diaz and Troy Schulze, Skyworks Solutions Inc.

3:30 PM **10.2 Characterization of Arsenic-Rich Waste Slurries Generated During Gallium Arsenide Wafer Lapping and Polishing**
H.E Keenan[1], J. Sefcik[1], A. Hursthouse[2] and K.W Torrance[1].
[1]University of Strathclyde, Glasgow;
[2]University of the West of Scotland, Paisley.

3:50 PM **10.3 Improving Organizational Performance through Goal Deployment**
James Oerth and Andy Hunt, Skyworks Solutions Inc.

4:10 PM **10.4 Web Based Business Intelligence for Semiconductor Manufacturing**
Leo F. Sennott, Skyworks Solutions, Inc.

4:30 PM **10.5 Cycle Time and Cost Reduction Benefits of an Automated Bonder and Debonder System for a High Volume 150 mm GaAs HBT Back-end Process Flow**
Dave Kharas and Nagul Sooriar, Anadigics Inc.

5;30 PM **RUMP SESSION RECEPTION**

6:00 PM **RUMP SESSIONS**

Chair: Yohei Otoki, *Hitachi Cable Ltd.*

SESSION A: CS on silicon technology – this time it's for real?
Moderator Kamal Alavi, Raytheon Systems

SESSION B: Is there a solar bubble?
Moderator: Marty Brophy, TriQuint Semiconductor.

SESSION C: Is GaN too hot?
Moderator: Drew Hanser, Kyma Technologies Inc.

SESSION D: **Automotive power electronics: GaN to the rescue?**
Moderator: Karim Boutros, HRL

7:00 PM **SEMI STANDARDS MEETING**

7:30 PM **CHAIRMANS EVENING**
SideBern's
2298 W. Morrison Ave.

Thursday May 21st

SESSION 11: MANUFACTURING

Chair: Andreas Eisenbach, *IQE Europe*

8:00 AM **11.1 In-Situ Monitoring of HBT Epi Wafer Production: The Continuing Push for Perfect Quality and Yields**
E. M. Rehder, K. Tsai, P. Rice, C. R. Lutz, and K. S. Stevens, Kopin Corp.

8:20 AM **11.2 HBT Epitaxy Material Matching and Qualification for High Volume Production**
Mike Sun, Peter Zampardi, Cristian Cismaru, and Lance Rushing, Skyworks Solutions Inc.

8:40 AM **11.3 Dramatic Reduction of Surface Defects and Particles on PHEMT Epi-Wafers Grown by MOVPE for Higher Yield of Transistors**
Hiroyuki Kamogawa, Hisataka Nagai, Kazuto Takano and Yohei Otoki Hitachi Cable Ltd.

9:00 AM **11.4 PHEMT Switch Yield Improvement through Feedback From 100% Die Test**
Min-Chang Tu, Paul Yeh, Shin-Ming Liu and Wei-Der Chang, WIN Semiconductors Corp.

9:20 AM **BREAK**

SESSION 12: DEVICE TECHNOLOGY

Chair: Tom Low, *Agilent Technologies*

9:40 AM *Invited Presentation*
12.1 Advanced GaAs MMICs Fabrication Process with PIN Diodes for ESD Protection
Kaoru Miyakoshi, Takehiko Kameyama, and Koichi Nagata, New Japan Radio Co.

10:10 AM **12.2 Monolithically Integrated GaInP/GaAs High Voltage HBTs and Fast Power Schottky Diodes for Switch-Mode Amplifiers**
P. Kurpas, A. Wentzel, B. Janke, C. Meliani, W. Heinrich and J. Würfl, Ferdinand-Braun-Institut für Höchstfrequenztechnik (FBH)

10:30 AM *Invited Presentation*
12.3 Device Technology Based on New III-N Heterostructures
Masaaki Kuzuhara, Graduate School of Engineering, University of Fukui.

11:00 AM **12.4 0.15 Micron Optical Gate 6" Power pHEMT Technology**
Cheng-Guan Yuan, Jean Sun, Jeff Huang, Rex Wu, Frank Chen, S.M. Joseph Liu and Der-Wei Tu, WIN Semiconductors Corp.

11:20 AM **12.5 Recessed JPHEMT Technology for Low Distortion and Low Insertion Loss Switch**
Shinichi Tamari, Koji Wakizono, Yuji Ibusuki and Mitsuhiro Nakamura, LSI Device Technology Department, Sony Semiconductor Kyushu Corporation.

11.40 AM **BREAK**

SESSION 13: PROCESS SPECIAL TOPICS

Chair: Victoria Williams, *TriQuint Semiconductor*

1:00 PM **13.1 Six-Sigma Methodologies Support Back-End Yield and Quality Metrics Improvement**
Tom Hand, Jennifer Welborn, and Jim Oerth, Skyworks Solutions Inc.

1:20 PM **13.2 Self-aligned Field-Plate PHEMT for 5.8 GHz Operation**
C.E. Weitzel, K. Moore, M. C De Baca, J-H. Huang, O. Hartin, J. Cotronakis, H. Stewart, S. Shaw, C. Gaw, T. Arnold and M. Miller, Freescale Semiconductor

1:40 PM **13.3 Effects of Ohmic Metal on Electrochemical Etching of GaAs in pHEMT Manufacturing**
Kezia Cheng, Skyworks Solutions Inc.

2:00 PM **13.4 Optimization of Bi-layer Lift-Off Resist Process**
Jeremy Golden, Harris Miller, Dan Nawrocki and Jack Ross, MicroChem Corp.

SESSION 14: OPTICS AND EMERGING TECHNOLOGIES

Chair: Shyh-Chiang Shen, *Georgia Tech University*

1:00 PM *Invited Presentation*
14.1 Manufacture of Sb-Based Type II Strained Layer Superlattice Focal Plane Arrays
Meimei Tidrow,[1] Lucy Zheng [2], Hank Barcikowski [3] James Wells [3] and Leslie Aitcheson [4]
[1]US Army RDECOM CERDEC NVESD, Ft. Belvior, VA [2]Institute of Defense Analysis, [3]Missile Defense Agency, [4]Computer Sciences Corp.

1:30 PM **14.2 Low Threshold Current Density InAs Quantum Dash Lasers on InP Using Double Cap Technique**
D. Zhou[1], B.O. Fimland[1], R. Piron[2], O. Dehaese[2], F. Grillot[2], S. Loualiche[2]
[1]Dept. of Electronics and Telecommunications, NTNU, [2]UMR-FOTON

1:50 PM **14.3 Monolithically Integrated III-V and Si CMOS Devices on Silicon on Lattice Engineered Substrates (SOLES)**
J.R. LaRoche[1], T.E. Kazior[1], W. E. Hoke[1], D. Lubyshev[2], J. M. Fastenau[2], W. K. Liu[2], M. Urteaga[3] W. Ha[3] J. Bergman[3], M. J. Choe[3], M. T. Bulsara[4] E. A. Fitzgerald[4], D. Smith[5], D. Clark[5] R. Thompson[5], C. Drazek[6] N. Daval[6], L. Benaissa [7] and E. Augendre[7], [1]Raytheon Integrated Defense Systems, [2]IQE Inc., [3]Teledyne Scientific Company, [4]Department of Materials Science and Engineering, Massachusetts Institute of Technology [5]Raytheon Systems Limited, [6]SOITEC, [7]CEA-LETI, MINATEC

2;10 PM **14.4 Technology for Dense Heterogeneous Integration of InP HBTs and CMOS**
Y. Royter, P.R. Patterson, J.C. Li, K.R. Elliott, T. Hussain, M.F. Boag-O'Brien, J.R. Duvall, M.C.Montes, D.A. Hitko, M. Sokolich, D.H. Chow and P.D. Brewer HRL Laboratories LLC

SESSION 15: INTERACTIVE FORUM

Chair: Suzanne Combs, *TriQuint Semiconductor* & Mike Clausen, *PETEC*

2:30 PM--4.00 PM

15.1 Semiconductor Industry - RCRA Air Emission Equipment Leak Standards"
Sara Burson and Danny Kringel, ERM

15.2 Paradigm Shift in Compound Semiconductor Production since the Introduction of Laser Dicing
Rene Hendriks, Jeroen van Borkulo and Mark Mueller, Advanced Laser Separation International (ALSI)

15.3 Use of FMEA methodology in Evaluation of Process Transfer of Ohmic Liftoff from Low Pressure Solvent to High Pressure NMP Liftoff
J.W.Crites and S.W.Kittinger, Cobham Roanoke

15.4 150 nm InP HBT Process with Two-Level Airbridge Interconnects and MIM Capacitors for Sub-Millimeter Wave Research
William Snodgrass, Mark Stuenkel, and Milton Feng, Univ. of Illinois.

15.5 The Effect of Chemical Treatment and Storage Time on the Surface Chemistry of Semi-Insulating Gallium Arsenide
Thomas Mirandi[1] and Douglas J. Carlson[2]
[1]Wafer World, [2]Cobham

4.00 PM **CONFERENCE CLOSING RECEPTION**

SESSIONS 1,2: PLENARY SESSIONS

Chair: Steven Mahon, *TriQuint Semiconductor*

The last year has seen a broad worldwide economic recession take hold. Historically, the semiconductor business sector has seen multiple boom and bust cycles, and we are similarly reeling with the rest of the world. Will this downturn be stronger and longer than those previously experienced by the industry? All this comes after a period of strong, broad growth in compound semiconductors for consumer electronics, solar power, infrastructure electronics, optical devices and military hardware. Wireless applications represent one of the strongest growth areas with amazing devices appearing almost daily. What will be the effect of the economic downturn on this area of our business? Earl Lum of EJL Wireless will attempt to shed some light with "The Impact of the Financial Crisis on the Compound Semiconductor Industry" In the military sector, there has been strong emphasis on GaN development and it has received a great deal of attention from the U.S. Government. We are honored to have Mark Rosker return, who will give us a summary of the progress of Phase II of the DARPA Wide Band Gap Semiconductor for RF Applications (WBGS-RF) Program. Before the break, we will receive an overview of the opportunities in concentrating photovoltaics and its competitive position with respect to other solar power technologies that currently dominate the market. Sara Kurtz of the National Renewable Energy Laboratory (NREL) will share with us the state of this emerging industry and its competitive position and future prospects, This paper will provide an excellent lead-in to the Solar Technology session later in the afternoon.

After coffee, three other outstanding papers will be presented. We begin with Tetsu Kachi of the Toyota Central Labs who will give us a top level perspective of wide band gap devices and their future in the automotive market. With the growth of alternative energy vehicles this paper will be one of great interest to the CS community. Following will be Bill Vassilakis of Powerwave Technologies contrasting LDMOS and GaN technologies for future use in the next generations of wireless base stations. Will LDMOS maintain its long standing hold or will compound technologies have their day in the sun? Finally, C.C. Chang of WIN Semiconductor will tell us what it takes to succeed in a pure compound semiconductor foundry. WIN has established a track

record for its GaAs foundry in the past few years, no doubt due to it's strong engineering and savvy business practices.

The CS MANTECH conference would like to thank these authors and those of the following sessions for their contribution to the collective knowledge of the industry.

SESSION 3: SOLAR CELLS

Chair: Noren Pan, *Microlink Devices*

This session covers a variety of topics related to CS Solar cell manufacturing. The contributed paper by Schneller et. al of Aixtron discusses the key aspects of MOCVD production that impact costs. An efficient usage of the source material, high growth rates, and large wafer diameters are critical factors in solar cell production. Sherif of eSolar describes the advantages of concentrated photovoltaics and future market opportunities of this technology. The semiconductor material usage is significantly decreased as the concentration factor is increased which provides a market opportunity for GaAs based materials. Takamoto of Sharp provides an overview of the current status of various solar cell technologies. Solar cells based on Ge substrates are currently used for the majority of high efficiency solar panels for satellite applications. Research on high efficiency solar cells will be covered including inverted metamorphic, quantum dots, and wider bandgap solar cells based on nitride materials. Wohlmuth of First Solar will provide an update on very low cost CdTe based solar cells, which are in direct competition with Si based solar cells for flat panel applications. CdTe materials can be produced at relatively low cost using simple deposition technology on glass or metal substrates.

SESSION 4: RELIABILITY/TEST

Chairs: Paul Werbaneth, *Tegal Corporation* & Mike Sun, *Skyworks Solutions*

Environmental factors such as electrostatic discharge or variations through wafer processing can significantly affect device reliability and robustness. For instance, poor quality silicon nitride films used in MIM capacitors can show up either as unexpected field failures and customer returns, or as yield losses during in-house electrical testing. "Belt-and-suspenders" overkill testing, while ensuring that only the known good devices go out

the door, adds significant costs to the finished devices. Alternatively, unexpected field failures from lightly-sampled shipped products can be devastating to future business. The papers in this Test and Reliability session address manufacturing-driven device reliability, the reliability of testing methodology, and the results from novel testing methods, to provide a better understanding of the performance and reliability of MIM capacitors, RF switches, and high frequency transistors. In the first paper, Anadigics describe how they measured the performance characteristics and physical properties of silicon nitride films deposited for MIM capacitor applications, and how their investigative efforts led to improved reliability for InGaP/GaAs HBTs. In the second paper, students from the Massachusetts Institute of Technology report on their work measuring and modeling the reliability of SiN MIM capacitors for high voltage – high temperature GaN MMIC applications. To identify and reduce variations in RF test results at the third harmonic for high performance, multi-throw RF switches, Skyworks Solutions performed a thorough Gage study in order to quantify measurement reproducibility and repeatability that resulted in a significant reduction in re-test. The fourth paper in this session, from United Monolithic Semiconductors, relays the development of a novel high frequency wafer level reliability test bench capable of providing short feedback loop information (and thereby shortening time-to-market) for MESFET, low noise and power pHEMT, HBT, and GaN HEMT process development. The Test and Reliability session finishes with a talk from the Fraunhofer Institute on Transmission Line Pulsing as applied to understanding and characterizing the Electrostatic Discharge robustness of broad band LNA circuits, and for capacitors fabricated in GaAs technology.

SESSION 5: GaN DEVICES

Chairs: Andy Souzis, *II-VI Corp.* & Robert Sadler, *Nitronex Corp.*

In this session we will be focusing on some of the latest advances in GaN devices. Our first two papers are concerned with substrate-related issues. First, Toshiba will report on the results of a study investigating the performance dependence of AlGaN/GaN HEMT's fabricated on SiC substrates with various mis-cut angles. In the second paper, United Monolithic Semiconductor (UMS) will examine the manufacturing aspects of backside via processing in thinned SiC substrates. Results utilizing either an ICP etch or an excimer laser at two different wavelengths will be compared. The remaining three papers describe a range of new GaN device technologies.

In the first, a team from the University of Florida and SVT Associates will report their demonstration of AlN/GaN transistors featuring an ultra-thin gate oxide layer obtained by UV ozone treatment of the AlN. In the next paper, a group from Auburn University will describe a biosensor for DNA hybridization. Based on an AlGaN/GaN transistor with three metalized contacts, the biosensor can provide rapid identification without labeling of samples before analysis. The last paper, from Hong Kong University of Science and Technology, will report the development of a stable voltage reference and a temperature-compensated comparator, both fabricated with a planar GaN-on-Si HFET process that enables a GaN smart power chip technology.

SESSION 6: PROCESS, METALIZATIONS

Chairs**:** Russ Westerman, *Oerlikon* & Thorsten Saeger, *TriQuint Semiconductor*

Papers in this session focus on practical problems that arise during the metallization of compound semiconductors and the solutions used to overcome them. The first paper of the session, a collaboration between the Air Force Research Laboratory and SVT Associates, compares the performance of various processes to form ohmic contacts for AlN/GaN MOSHEMTs. The second paper in the session by National Chiao-Tung University investigates the use of Cu-containing ohmic contacts for InGaP/GaAs HBTs. Device performance data comparing identical device structures with either Cu or Au based ohmics will be presented along with reliability data for the new Cu-based metallization. The next paper by Skyworks Solutions also looks at the potential of integrating Cu metallization into GaAs devices. In the paper, an evaporation process for the formation of Cu interconnects for pHEMT devices is described along with performance and reliability data from the new structure. In the fourth presentation, Cobham looks at improving process control of refractory metal deposition for thin film resistor and gate applications. The paper examines the relationship between the deposited film properties, process responses and equipment performance to isolate a root cause of process variability and minimize it. In the final presentation of the session GAETEC looks at the metallization requirements for GaAs based RF MEMs switch applications. The paper investigates different metallization processes and switch configurations in an effort to optimize RF switch performance.

SESSION 7: PROCESS/ETCH

Chairs: Michelle Bourke, *Surface Technology Systems* & Scott Sheppard, *Cree Inc.*

The traditional process session begins with an exciting paper from Fujitsu Limited and Fujitsu Laboratories Ltd. The paper discusses the process optimization of SiC Via-holes for GaN HEMT MMIC devices resulting in a via that is etched at 2µm/min. The first TriQuint paper in the session is from the Oregon facility and introduces the new TriQuint process called the TQP25 – the combination of the 0.25µm DFET with a 0.35µm EFET using optical stepper technology in AlGaAs/ InGaAs. Moving to their Texas facility, the second TriQuint paper reviews the process optimizations that must take place to ensure systematic pillar formation will be avoided in SiC via holes for high power MMIC devices. The final TriQuint paper is from the Oregon facility and reviews the influence of different dielectric plasma etch sources on pHEMT device performance. This process session then concludes with a paper from the National Chiao Tung University in Taiwan. The paper presents the RF-via and flip chip bump transitions for applications of packaging microstrip RF- MEMS devices. A novel fabrication process for the packaging of RF MEMS devices will also be demonstrated.

SESSION 8: RELIABILITY, THERMAL ANALYSIS

Chair: Peter Ersland, *Cobham*

The importance of device temperature on product performance and reliability is well known, however challenges remain in accurately determining these temperatures. The five papers included in this session discuss techniques for measuring device temperature, compare the results of these techniques with one another, and consider some of the implications of elevated device temperature. Four of these papers are written by students, and all use Raman spectroscopy in addition to other techniques for temperature characterization.

The first paper from Claflina et al combines temperature measurement with finite-difference models to understand the mechanical stresses present in AlGaN/GaN HFETs grown on various substrates and as a function of applied drain voltage. Next, Hosch et al report that even under constant power dissipation conditions, drain voltage has a significant impact on the temperature distribution within an AlGaN/GaN HEMT. The third paper, from Wang et al describes the use of micro-Raman and electroluminescence spectroscopies to characterize the operating temperature of GaN-based LEDs. The next

paper from Xu et al again uses micro-Raman spectroscopy, this time for temperature characterization of high-power Schottky diodes manufactured on free-standing GaN-based materials. The fifth and final paper of the session, from Sarua et al compares device temperature distributions given by IR imaging, micro-Raman spectroscopy, micro-photoluminescence spectroscopy, and thermal modeling. The implications of the temperature differences provided by these techniques on predicted device reliability will be presented.

SESSION 9: GaN GROWTH AND CHARACTERIZATION

Chairs: John Blevins, *AFRL/RXPS* & Ruediger Schreiner, *Aixtron AG*

This session reviews the latest progress in techniques for growth and characterization of bulk GaN and the use of PVD based AlN nucleation layers for LED manufacturing. A multi-disciplinary group from Radboud University Nijmegen and the Polish Academy of Sciences will review their use of hydride vapor phase epitaxy (HVPE) for growth of free standing GaN substrates taking advantage of spontaneous lift-off from its seed crystal. Kyma Technologies will describe the production challenges for manufacturing bulk GaN substrates and the control of their physical and geometric properties, focusing on the mis-cut angle and direction of the substrate. North Carolina State University will report on the effect of HVPE grown low dislocation density bulk GaN on the thermal conductivity. Finally, Kyma Technologies will report on use of PVD grown AlN nucleation layers to improve LED manufacturing and cost structure.

SESSION 10: FAB MANAGEMENT

Chair: Alex Smith, *Brewer Science, Inc*.

In this session the speakers explore a variety of aspects of CS fab management and improvement.

In the first talk, Skyworks Solutions describe how a robust Environmental Management System is a key component to running a green fab. Strategic tracking of manufacturing process improvements enables a reduction in the environmental impacts of the fab The second talk of the session is by the University of Strathclyde, and University of the West of Scotland, and addresses a specific III-V fab waste stream contaminate namely arsenic. The authors discuss the characterization of arsenic rich waste slurries generated during gallium arsenide wafer lapping and polishing. The analytical results of the study provide manufacturing guidance as to the most effective

strategy to minimize the environmental impact of slurries produced during wafer thinning and polishing.

The third presentation covers fab management, Skyworks Solutions relay how they are improving organizational performance through goal deployment.

The forth talk also by Skyworks Solutions shifts gears to focus on web based business intelligence in semiconductor manufacturing. This paper presents a series of business intelligence solutions required for the seamless manufacturing of FEM's and all of Skyworks wireless semiconductor products.

In the fifth and final paper in the session, Anadigics shares a significant GaAs HBT back-end process flow improvement. Anadigics shares how they were able to reduce cycle time and cost by utilizing the benefits of an automated bonder and debonder system in their high volume 150 mm fab.

SESSION 11: MANUFACTURING

Chair: Andreas Eisenbach, *IQE*

Manufacturing excellence and yield (and concerns about both) are at the very core of CS MANTECH. The presentations in this session cover two major compound semiconductor building blocks of the wireless industry, HBTs and pHEMTs, and link yield improvement and cost reduction to improved hardware, manufacturing, material selection, and testing processes. Several aspects from basic materials to final testing are shown to improve manufacturing efficiency in today's modern compound semiconductor wafer fabs.

The presentation from Kopin attempts to bridge the ever-problematic data gap between non-destructive epi-wafer characterization and full-scale destructive testing by device fabrication/measurement. By introducing In-Situ monitoring during the growth of HBTs they show that problems can be detected early and corrective actions taken, thus, ensuring better consistency and yields,. In an even earlier stage of the growth process, Hitachi Cable's paper demonstrates that careful hardware optimization – particularly with respect to temperature distribution within the reactor – can significantly reduce surface defects and particles on pHEMT epi-wafers grown by MOVPE, thus improving yields in device manufacturing.

On the device side, Skyworks' presentation demonstrates the need for, and success of, an efficient epi qualification process that places strong emphasis on matching of existing production qualified materials. They discuss procedures and case studies that allow efficient qualification across multiple reactors and suppliers to support the rapidly changing market place. Last but not least, smart and efficient testing can greatly help to reduce

cost and improve yields by shortening feedback times and by unmasking process drifts and failure mechanisms. This is presented in the paper by WIN on pHEMT yield improvement through incorporation of a wafer-level die test in addition to the customary automatic visual inspection

SESSION 12: DEVICE TECHNOLOGY

Chair: Tom Low, *Agilent Technologies*

The session begins with an invited paper from Kaoru Miyakoshi-san of New Japan Radio Co. on using optimized GaAs PIN diodes for ESD protection of GaAs HFET MMICs. The resulting GaAs HFET MMICs are robust to ESD and survive up to 2000V when the ESD is applied via the human body model. The second paper from P. Kurpas of the Ferdinand-Braun-Institute describes the integration of 'high-voltage' power HBTs with fast, high-voltage blocking Schottky diodes for use in switch-mode power amplifiers. The resulting Schottky diodes have high breakdown voltages, similar to the power HBT (~70V), and much shorter recovery times (12ps) than the p-n junction alternative. The third paper is another invited paper by Masaaki Kuzuhara-san from the Graduate School of Engineering of the University of Fukui. Dr. Kuzuhara will present a paper on “Device Technology Based on New III-N Heterostructures”. The fourth paper of the session is from WIN Semiconductors Corp, and describes their 0.15 um Optical Gate 6” Power pHEMT Technology which is ready for high volume low cost production at WIN. The process uses i-line lithography to write the gates followed by re-flow operation to shrink them to 0.15µm on 6” diameter wafers. The paper describes the process flow and reports on the excellent yield of this new process. The final paper in this session is presented by Shinichi Tamari-san of the LSI Device Technology Department of Sony Corporation. The paper describes a novel recessed JPHEMT technology for fabrication of low distortion and low insertion loss switches on 6” GaAs wafers which is compatible with high volume production. The excellent Ron and Coff characteristics of this technology are presented along with data on RF IMD products quantifying the good linearity achieved with stacked FETs.

SESSION 13: PROCESS SPECIAL TOPICS

Chair: Victoria Williams, *TriQuint Semiconductor*

Finding solutions to process issues is fundamental to the manufacturing capability of compound semiconductor organizations. This session highlights

process investigations that are designed to improve either yield or performance or that are directed at optimizing process flow. The session will start with a paper by T. Hand, et. al. from Skyworks Solutions, who report on the use of six sigma methodologies to understand the cause of yield loss in backend processing and, thereby, utilize process improvement strategies to demonstrate a steady increase in backend process yield over three years. The second presentation will be one by C.E. Weitzel, et al. from Freescale Semiconductor, describing the epi structure, design investigation, and process flow that enabled 5.8GHz operation of a GaAs pHEMT using a self-aligned second field plate. This is followed by a study of the effect of different metal compositions on galvanic etching of ohmic contacts on GaAs during wet processing steps, reported by K. Cheng of Skyworks Solutions. The session concludes with a paper by J. Golden and co-workers at MicroChem Corporations, describing the optimization of key process parameters for improving the resolution of a LOR/PMGI bi-layer resist process.

SESSION 14: OPTICS AND EMERGING TECHNOLOGIES

Chair: C.S. Shen, *Georgia Tech University*

This session will start with an invited presentation on the manufacture of Sb-based type-II strained layer superlattice focal plan arrays by Dr. Meimei Tidrow. The presentation will discuss the advantages of Sb-based type II strained superlattice over HgCdTe counterparts and current technology development progress. A paper focusing on a demonstration of low threshold current density InAs lasers will also be presented by colleagues from NTNU, Norway. The session will then switch gears to focus on emerging technologies that promise to integrate compound semiconductor devices with silicon CMOS. Colleagues from HRL Laboratories will first describe a novel technology for dense heterogeneous integration of InP HBTs and CMOS that maintains maximum CMOS integration density and HBT performance, while keeping the heterogeneous interconnect length below 5um. A paper from Raytheon will also reveal a monolithic integration approach for III-V and Si CMOS devices using innovative silicon on lattice engineered substrates (SOLES) technology.

Special Thanks to our 2008 Exhibitors

Accel-RF
Air Products
AIXTRON
AxRTech
AXT, Inc.
Brewer Science
Bridgestone Corporation
Bruker AXS Inc.
China Crystal Technologies Co., Ltd
Cree, Inc.
Design Workshop Technologies Inc.
Diamond Wire Technology
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Hitachi Cable Ltd.
HOLOGENIX INC.
ICOS Vision Systems, Inc.
II-VI Incorporated, Wide Bandgap Materials Group
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Reedholm Instruments
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(Continued on next page)

Special Thanks to our 2008 Exhibitors (continued)

SAES Pure Gas, Inc.
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Vistec Electron Beam GmbH
Visual Photonics Epitaxy Company
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WEP
Williams Advanced Materials
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GENERAL INFORMATION

2009 International Conference on Compound
Semiconductor Manufacturing Technology
May 18th – May 21st, 2009
Tampa Marriott Waterside Hotel and Marina
700 South Florida Avenue
Tampa, Florida 33602

REGISTRATION INFORMATION (US$)

Register for the conference online at our Web Site:
www.csmantech.org

	On or before Apr. 16th	After Apr 16th
Full Conference Registration	$525.00	$625.00
Student Conference Registration	$125.00	$125.00
Government Conference Registration	$525.00	$525.00
One-Day Conference Registration	$300.00	$300.00
Workshop Registration	$300.00	$400.00
Government Workshop Registration	$300.00	$300.00

Payment of the full, student, or government conference registration fee includes one copy of the printed Conference Digest (if desired), one copy of the Conference Digest on CD, and admission to all sessions and the Exhibits. It also includes the International Reception, Exhibits Reception, Exhibits Luncheon, Panel & Rump Session Reception, Interactive Forum Reception, continental breakfasts, and refreshment breaks. Additional copies of the Conference Digest may be purchased at $150.00 each. Additional copies of the Conference Digest on CD may be purchased for $50.00 each.

The one-day registration includes admission to all sessions for that day, admission to the Exhibits Hall, continental breakfast, refreshment breaks, and lunch. The Rump Session Reception or Interactive Forum Reception is included on Wednesday and Thursday, respectively. It also includes a printed Conference Digest and a Conference Digest on CD. The one-day registration does *not* include admission to the International Reception. The one-day option can be taken only once during the conference.

Payment of workshop registration includes one copy of the Workshop Digest, continental breakfast, Workshop Luncheon and refreshment breaks. Additional copies of the Workshop Notes may be purchased at $100.00.

For Advanced Conference Registration, please visit our website www.csmantech.org or complete the enclosed

Registration Form at the end of this Advance Program and return with payment by April 16th to:

CS MANTECH
14525 SW Millikan Way #26585
Beaverton, Oregon 97005-2343

Registrants may pay by check, or credit card. Make checks payable in U.S. dollars drawn on a U.S bank to: "CS MANTECH, Inc." Your name and address must appear on the check. The only acceptable credit cards are Master Card, VISA, and American Express. REGISTRATION FORMS SENT WITHOUT PAYMENT WILL NOT BE ACCEPTED. All refund requests must be received shown below by April 16th for a full refund less a $25 processing fee. **NO REFUNDS AFTER APRIL 16th.**

HOTEL RESERVATIONS

A block of rooms at the Tampa Marriott Waterside has been reserved for CS MANTECH participants and their guests. The special CS MANTECH room rate is $169.00 for single or double occupancy. Occupancy taxes (currently 12%) will be added to these rates.

Hotel reservations may be made through our website *www.csmantech.org*

Reservations can also be made by calling toll free: 1-888-268-1616 within North America. Please be sure to mention you are a CS MANTECH attendee.

If needed, a Hotel Reservation Form is available at www.csmantech.org that can be mailed directly to the Hotel.

All reservations must be guaranteed with a credit card, or a cash advance. A deposit equal to one night's stay is required to hold each reservation. The deposit is refundable if notice is received at least forty-eight (48) hours prior to scheduled check-in. One night's room and tax will be charged if cancelled less than 48 hours prior to arrival.

Please support CS MANTECH and enjoy all of the conference activities by staying at our official 2009 location. CS MANTECH has worked with The Tampa Marriott Waterside to provide the optimum convenience

and value for conference attendees.

Hotel reservations must be received BEFORE April 16th, 2009 to qualify for a room in the CS MANTECH room block. The discounted rate is subject to availability, so please MAKE YOUR RESERVATION EARLY!

Reservations received after April 16th, 2009 will be accepted on a space- and rate-availability basis.
If the room block fills prior to the cut off date, reservations will be accepted based on space and rate availability, so RESERVE EARLY!

CONFERENCE REGISTRATION & INFO CENTER

Conference registration will open at Office 1 & 2 on the second floor of the Tampa Marriott Waterside on Sunday night and will be open Monday through Thursday. Please refer to the "Conference At A Glance" for specific hours of operation. A Conference Attendee list will be available at the Information Center on Thursday, May 21st.

SPEAKER PREPARATION ROOM

Meeting room 7 on the Second floor has been reserved for speaker preparation. This room will be open from 7:00 am to 5:00 pm on Monday through Thursday, May 18th-21st. The room will be set up with appropriate previewing equipment.

THE CONFERENCE HOTEL

The Tampa Marriott Waterside Hotel and Marina located in downtown Tampa, is part of the Channelside District, a region known for its nightlife, restaurants, shopping and entertainment. The Tampa Aquarium is located about a half mile away, while Busch Gardens, Lowry Park Zoo, and Ybor City are within easy driving distance.

The Tampa Marriott Waterside features over 700 newly renovated rooms, each equipped with a spacious work desk with dual-line speakerphones, voicemail, and a data port offering high-speed wireless internet service. A hospitality center in each room includes a mini-bar and coffeemaker. Iron/ironing board and hair dryer are also standard in all rooms. The business center in the hotel offers copying and faxing services. The concierge service is eager to assist you with your needs. Food and beverage amenities and services include three restaurants, a lobby bar (open until midnight) and 24-hour room service.

A full service spa and a complete fitness center provide opportunities for both relaxation and workouts. Spa services include massages, manicures, pedicures, facials, body wraps, and a variety of special treatments. An outdoor pool and Jacuzzi® are also available. Several golf courses are within 15 miles, and water skiing, kayaking, and snorkeling are nearby. In addition to being a luxurious hotel, the Tampa Marriott Waterside has a 32-slip, full-service marina. So if you prefer not to fly to the conference, it is also possible to arrive by yacht..

For more detailed information on the Tampa Marriott Waterside, visit www.marriott.com or click on the hotel link at www.csmantech.org.
For more information on Tampa activities, visit
http://www.visittampabay.com or
http://www.tampaguide.com

TRANSPORTATION TO THE HOTEL

The Tampa Marriott is easily reached in about 15 minutes from the Tampa International Airport.

Taxi: Taxis are available at the airport. Taxi rates from the airport to the Tampa Marriott are approximately $25.00.

DRIVING DIRECTIONS

From Tampa International Airport: Exit the airport, turning right on N. West Shore Blvd, immediately left onto W Ohio Ave. Turn right onto N Lois Ave. At the roundabout, take the second exit onto W Tampa Bay Blvd. Turn right onto US 92, and then take the ramp onto I-275. At exit 44, take the ramp on the right. Keep left on the ramp, which becomes E Scott St. Turn right onto Morgan St, right again onto St. Pete Times Forum Dr. then immediately bear right onto S. Florida Ave. The hotel is at 700 S. Florida Ave.

Parking at the Hotel: $18 per night

FINANCIAL ASSISTANCE

CS MANTECH strongly encourages and supports participation from academic delegates. Students and University Professors seeking financial assistance should contact Drew Hanser, the 2009 University Liason, by email at student.aid@csmantech.org.

2009
MANTECH
Registration Form

Please register on line at
www.csmantech.org

OR mail the attached Registration form to: (*Please note the new mailing address for 2009)*

CS MANTECH, Inc.
14525 SW Millikan Way #26585
Beaverton, Oregon 97005-2343

Registration Fees: *Includes one printed copy and one CD of the Conference Digest, admission to all sessions, Exhibit Hall, International and Exhibits Receptions, Exhibit Luncheon, Panel & Rump Session Reception, Interactive Forum Reception, continental breakfasts and refreshment breaks. (All fees in US$.)* ***EXCEPT FOR STUDENTS, CONFERENCE REGISTRATION FEE DOES NOT INCLUDE WORKSHOP REGISTRATION FEE.***

Full Early Registration through April 16th .... $525 $_____
Full Registration after April 16th..... $625 $_____
One Day Registration* ..... $300 $_____
Check one: *May 18th*____ or *May 19th* ____ or *May 20th* ____
Government Registration**..... $525 $_____
Student Registration (includes Workshop) ... $125 $_____
Additional Copies of Conference Digest-$150 each $_____
Additional CDs of Conference Digest-$50 each $_____
Additional Tuesday Night International
Reception Tickets #_____..... $50 each $_____

2009 Workshop on May 18th:
Includes one copy of the Workshop Notes, continental breakfast, Workshop Lunch, and break refreshments
Workshop Early Reg. through April 16th ..... $300 $_____
Workshop Reg. after April 16th..... $400 $_____
Government Workshop Registration……..$300 $_____
Additional Copies of Workshop Notes-$100 each $_____

2009 Digest and Workshop Information*:**
2009 Conference Digests... #_____..... $150 each $_____
2009 Conference CD ..... #_____..... $50 each $_____
2009 Workshop Notes ..... #_____..... $100 each $_____

Total $_____

* One-Day Registration can be used only once during the Conference. It includes a copy of the Conference Digest and CD. It does not include admission to the International Reception.

** Must fax proof of government employment if registering after April 16th. Not for contractors.

*** Visit www.csmantech.org to order Conference Digests, Workshop Notes, or Workshop Videos for prior years.

Early Conference/Workshop Registration Cutoff Date
April 16th 2009

Conference Registration Form Continued

Please indicate which special events you plan to attend:

- ❑ Exhibits Reception (Monday evening)
- ❑ Exhibits Luncheon (Tuesday lunch)
- ❑ Exhibitors' Forum (Tuesday afternoon)
- ❑ International Reception (Tuesday evening)
- ❑ Panel & Rump Sessions (Wednesday afternoon)
- ❑ Interactive Forum (Thursday afternoon)

Please TYPE or PRINT clearly:

Name:_____

Badge Name:_____

Company:_____

Address:_____

City: _____ State: _____ Zip: _____

Country: _____

Phone: _____ Fax:_____

Email:_____

Payment must accompany registration form. Registration forms sent without payment will not be accepted. Requests for refunds (less $25 processing fee) must be made to address above by April 16th. No refunds after April 16th, 2009.

Payment: ❑ VISA ❑ MasterCard ❑ AMEX

Name on Card:_____

Card No:_____

Exp. Date:_____

❑ Check (payable to "CS MANTECH, Inc.")

Signature:_____

TAMPA MARRIOTT WATERSIDE

MEETING ROOM LAYOUT