2007
International Conference on Compound Semiconductor Manufacturing Technology

May 14 - 17, 2007

Register Online at
www.CSMANTECH.org

Hilton Austin,
Austin, Texas, U.S.A.

Photograph Courtesy of Austin CVB

CONFERENCE AT A GLANCE

SUNDAY, May 13

6:30 PM – 8:30 PM	REGISTRATION Salon H Prefunction

MONDAY, May 14

7:00 AM – 10:00 AM	REGISTRATION Salon H Prefunction
7:00 AM – 8:00 AM	Buffet Breakfast SALON G
8:00 AM – 5:00 PM	**WORKSHOPS** SALONS D, E
12:00 PM – 1:15 PM	**WORKSHOP LUNCHEON** SALON G
1:00 PM – 3:30 PM & 5:00 PM – 7:30 PM	REGISTRATION Salon H Prefunction
6:00 PM – 9:00 PM	**EXHIBITS RECEPTION** SALON H-J-K

TUESDAY, May 15

7:00 AM – 11:00 AM & 1:00 PM – 5:00 PM	REGISTRATION Salon H Prefunction
7:00 AM – 8:00 AM	Continental Breakfast SALON H-J-K
8:00 AM – 8:30 AM	**OPENING CEREMONIES**
8:30 AM – 10:30 AM	**SESSION 1: Plenary** SALON F-G
10:00 AM – 5:30 PM	**EXHIBITS OPEN** SALON H-J-K
10:30 AM – 11:00 AM	BREAK SALON H-J-K
11:00 AM – 12:30 PM	**SESSION 2: Backside Process I** SALON F-G
12:30 PM – 1:35 PM	**EXHIBITS LUNCH** SALON H-J-K
1:35 PM – 3:30 PM	**EXHIBITORS' FORUM I and II** SALONS F AND G
3:30 PM – 3:50 PM	BREAK SALON H-J-K
3:50 PM – 5:30 PM	**SESSION 3: Reliability** SALON F
3:50 PM – 5:30 PM	**SESSION 4: Devices & Models** SALON G
7:00 PM – 10:00 PM	**INTERNATIONAL RECEPTION** A fun-filled event of local flavor

WEDNESDAY, May 16

7:30 AM – 10:30 AM & 12:30 PM – 5:30 PM	REGISTRATION Salon H Prefunction
7:00 AM – 8:00 AM	Continental Breakfast Salon H Prefunction

8:00 AM – 9:50 AM	**SESSION 5: GaN Reliability and Testing** SALON F
8:10 AM – 9:50 AM	**SESSION 6: Etch and Clean** SALON G
9:50 AM – 10:10 AM	BREAK Salon H Prefunction
10:20 AM – 12:00 noon	**SESSION 7: Novel Substrates** SALON F
10:10 AM – 12:00 noon	**SESSION 8: Backside Process II** SALON G
12 noon – 1:00 PM	**OPEN LUNCHEON** ***Enjoy Austin!***
1:00 PM – 2:40 PM	**SESSION 9: Power Transistors** SALON F
1:00 PM – 2:40 PM	**SESSION 10: Frontside Process** SALON G
2:40 PM – 3:10 PM	Break Salon H Prefunction
3:10 PM – 4:40 PM	**SESSION 11: GaN & SiC Power Devices** SALON F
3:10 PM – 4:40 PM	**SESSION 12: III-V MOSFETs** SALON G
6:30 PM – 7:30 PM	**Rump Sessions** Meeting rooms 406, 408, 410, 412, SALON D, E
7:30 PM – 9:00 PM	SEMI STANDARDS MEETING Meeting Room 406

THURSDAY, May 17

7:30 AM – 9:30 AM	REGISTRATION Salon H Prefunction
7:00 AM – 8:00 AM	Continental Breakfast Salon H Prefunction
8:00 AM – 10:00 AM	**SESSION 13: BiFET Technology** SALON F
10:00 AM – 10:30 AM	BREAK Salon H Prefunction
10:30 AM – 12:10 PM	**SESSION 14: Manufacturing and Yield** SALON F
12:10 PM – 1:10 PM	**INTERACTIVE FORUM LUNCH**
1:10 PM – 3:10 PM	**SESSION 15: Interactive Forum** SALON G
3:10 PM – 3:40 PM	**RECEPTION & Conference Close**

MESSAGE FROM THE CONFERENCE CHAIR:

As Chair for the 22nd International Conference on Compound Semiconductor MANufacturing TECHnology and on behalf of the Technical Program Committee and Board, I would like to invite and encourage all practitioners in this technology to join us for our meeting. It will be held at the Hilton in Austin, Texas, USA, May 15-17, 2007, preceded by the Workshop on May 14.

Previous attendees of our conference will find that our Technical Program Committee (TPC) has again put together a Technical Program of first-rate papers covering the range of current activity in our dynamic industry. Our hard-working TPC includes over 60 volunteers from a broad spectrum across our industry of companies, research laboratories, universities, and funding agencies. This breadth assures we are up-to-date on the latest manufacturing techniques and trends and the outlook for emerging technologies.

Although our technical papers are of central importance, much more is offered. Monday's Workshop provides an opportunity to be brought up to date on a number of topics of broad interest. Tuesday features our Exhibits. Visitors learn about the latest products from companies serving our industry by visiting booths and by attending the Exhibitors' Forum Since its inception, a hallmark of CS MANTECH has been providing a wide range of opportunities for discussions, exchange of information, and networking in a relaxed, informal setting. Our social events, the Monday Exhibits Reception and Tuesday's International Reception, are a pleasant mix of business and fun. The Rump Sessions on Wednesday evening are a freewheeling, no-holds-barred discussion of technical issues. At the Interactive Forum on Thursday you can meet one-on-one with all our authors to discuss their work. Finally, in a break with the past, our Conference Close features a Most Beautiful Picture Contest.

Fortunately, current economic signs point to growth for our industry. Meeting future challenges will require being up-to-date on the latest in industry innovations. Join us! Let us learn from each other and have some fun as well! And please don't forget to complete your Feedback Form so we can continue to improve.

See you there!

George Henry
Conference Chair, 2007 International Conference on
Compound Semiconductor Manufacturing Technology

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(partial list, as of January 9, 2007)

MANTECH is an independent not-for-profit organization whose mission is to promote technical discussion and scientific education in the compound semiconductor manufacturing industry. The continued success of the conference is enabled by donations from corporate sponsors. The 2006 MANTECH Conference Committee gratefully acknowledges the support from our sponsors.

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CONFERENCE HIGHLIGHTS

MANTECH's 2007 Technical Program Committee has assembled an excellent program that includes 73 outstanding presentations on a wide variety of topics related to compound semiconductor manufacturing technology. The broad and worldwide scope of our industry is reflected by our mix of contributors. Over 40 industry, government, and university labs are represented. 26 (35 %) of our papers are international, and several cross national boundaries through collaboration of authors from various countries. In addition, 7 student papers are scheduled. Also, as is traditional for MANTECH, the strong technical program is augmented by a variety of social events, providing opportunities to network and build professional relationships and friendships.

Our week begins on Monday, May 14, with our Workshop. Workshop attendees may select from a total of 7 topics, running in two parallel sessions. Opening Session One will be a characterization tutorial followed by a series of two workshops, including space flight qualification procedures and a tutorial on intellectual property, areas of great interest to many. In the parallel session, a tutorial on high-speed and optical networks will first keep you engaged. This will be followed by two topics on SiC device processing and optimization for power switching devices: a SiC MOS tutorial and a historical overview of SiC material/device processing with a wide-bandgap introduction. Finally, a complete discussion of semiconductor device TCAD will increase your appreciation of the continuity equations and mesh optimization.

The Industry Exhibits feature many prominent suppliers to the compound semiconductor industry. The exhibits open on Monday evening with the first MANTECH social event, the Exhibits Reception. The exhibits continue all day Tuesday, when attendees may enjoy breakfast, morning and afternoon breaks, and the Exhibits Lunch while browsing the exhibit aisles. As was done last year, the Exhibitors' Forum will be held immediately following the Exhibits Lunch on Tuesday.

The technical sessions begin Tuesday morning, May 15, with the Plenary Session, which launches the conference with a keynote address on the state of our industry and follows with a review of the business in Europe. Then, overview presentations of solar cells and bulk acoustic wave devices move us from the business to the technical side of things.

Following the Plenary Session, the general Technical Sessions commence in parallel sessions Tuesday afternoon and all day Wednesday and in a single session on Thursday. These feature papers are presented by leading technologists and address many key areas of compound semiconductor technology: Manufacturing, HBTs, FETs, HEMTs, Wide Bandgap Technology, Processing, Materials, Reliability, Test, and Optoelectronics.

Of special note among the Technical Sessions are two "all invited" sessions. First, late on Wednesday Session 12 reviews the three extant approaches to III-V MOSFETs from leading researchers in that elusive technology. This is followed on Thursday morning by a comprehensive review of the leading fabs' approaches to mixing pHEMT or MESFETs with HBTs in one epi growth. This review of one of the hottest topics in our industry is sure to be worth getting up early for!

In addition, one side of Wednesday's parallel sessions focuses on wide bandgap applications including the realization of some truly impressive GaN and SiC device powers and breakdown voltages by companies from around the world. All this, plus our usual complement of fine papers on front- and backside fab, reliability, manufacturing, devices, and materials, makes this the one conference compound semiconductor technologists cannot miss each year!

MANTECH social events continue on Tuesday evening with the International Reception. Attendees will have a chance to network and enjoy a bit of Texas.

Wednesday evening features the popular Rump Sessions, complemented with snacks and drinks. Attendees may join any of the six parallel topics, where moderators will encourage informal, highly interactive, lively and informative discussions.

Traditionally one of the highlights of the conference, the Interactive Forum will be held on Thursday. This is a poster session containing papers on a diverse range of topics, as well as posters of all of the presented papers. It provides an excellent opportunity to meet with all the authors and to discuss the papers casually over drinks and snacks.

The conference ends with our Conference Closing Reception, which follows immediately after the Interactive Forum. At this time a raffle drawing for a fabulous prize will be held. All those who complete and submit their Feedback Forms will be entered. In addition, the Best Poster and Best Beautiful Picture Awards will be

presented, based on a vote of the attendees. And it will be a last chance to exchange business cards, discuss issues of mutual interest, and say good-bye until next year.

WORKSHOPS – New Lower Price!

Each year CS MANTECH provides many opportunities for sharing technical knowledge and learning from one another in an interactive environment. Be sure to take advantage of your first chance to do so by attending the workshop this year. **Note our new lower price ($100 off) for the workshops!**

The sessions will be presented on Monday May 14 by industry and university experts who have a wealth of knowledge and hands-on experience. You will improve your industry outlook and basic understanding of important items in various fields. Parallel sessions will be offered, covering a wide range of topics including semiconductor device space flight qualification, wide-bandgap processing, characterization, simulation and even intellectual property management. The workshop schedule can be found on page 18 of this Advance Program.

The first session will begin with “Surface and Thin Film Analysis for Compound Semiconductors” by Dr. Yumin Gao of Evans Analytical Group. This workshop will present many commonly used surface and thin film analytical techniques (SIMS, TOF-SIMS, RBS, Auger, XPS/ESCA, LEXES, TXRF, Raman/FTIR, etc.) and their applications in the compound semiconductors industry. After providing background knowledge of these techniques such as instrumentation and analytical conditions, Dr. Gao will describe their applications in materials research, process development, failure analysis, and production quality control through numerous examples in the areas of pHEMTs, HBTs, LEDs and LDs (GaAs, InP, GaN and SiC). This tutorial will increase your knowledge of analytical methods and your understanding of how these techniques can be applied most effectively to your specific problem solving and will provide a starting point for your further study.

Next, “Space Qualification for Semiconductor Devices” will be explained by Dr. Sammy Kayali of the NASA Jet Propulsion Lab. His tutorial will begin with a description of the environmental, reliability, and operational challenges for space applications. A description of space qualification requirements and associated product testing and evaluation will be presented. Semiconductor device processing, test, and characterization requirements along with supporting data and application support will also be

presented. To finish, Dr. Kayali will review practical considerations for development of qualification plans for space applications.

Then, by popular demand, Mr. Harvey Kauget will tell us all about the part of our business that scientists and engineers rarely understand. In "Intellectual Property: Know How and Why," Mr. Kauget will provide an overview of the basic forms of IP, developing an IP strategy, IP licensing and IP litigation issues. You will learn how to recognize and develop IP, and you will understand the issues of enforcing and/or licensing your IP.

In a parallel session with the above topics, three other highly interesting topics will be covered. First, Professor M. Kalam of the University of Texas at Dallas will describe in detail "High-Speed, Next-Generation Networks and the Role of the Semiconductor Industry". His workshop will begin with a background of various types of data and telecommunications networks and their evolution. The current networking technologies and the future trends will be discussed in detail. The contributions of the semiconductor industry in developing networking technologies will be elaborated. Dr. Kalam will discuss the close relationships that exist between the semiconductor industry and the networks of the future.

Following optical networks, there will be two wide-bandgap-related workshops. First, "Application of MOS Technology to Silicon Carbide Devices" will be presented by Dr. Mrinal Das of Cree, Inc. Silicon carbide (SiC) stands unique amongst the family of wide bandgap semiconductors due to the presence of a high quality, native oxide. Formed via thermal oxidation, this silicon dioxide layer opens the door to the vast legacy of MOS devices successfully developed on silicon (e.g., MOSFETs, DMOSFETs, UMOSFETs, LDMOSFETs, IGBTs, CCDs, DRAM, and CMOS circuitry). This workshop will cover the MOS fundamentals (kinetics, process technology, and characterization), including the pitfalls of simple application of Si MOS characterization to wide bandgap materials. Following this, Dr. Das will survey the historical progress and future potential of MOS-based silicon carbide devices to revolutionize power and microwave electronics.

Next, Professors Jim Cooper, Jr. and Mike Capano of Purdue University will survey silicon carbide material processing and high-voltage device design using a historical perspective. They will review the materials challenges involved in the fabrication of electronic devices in the wide-bandgap semiconductor silicon carbide.

Complex fabrication issues include ion implantation and activation, thermal oxidation, MOS properties, and the formation of Ohmic contacts. Material issues include defects and dislocations in epitaxial material, control of doping and surface morphology during epi growth, and point defects that limit the minority carrier lifetime. The payoff is new classes of circuits that can be fabricated with SiC unipolar and bipolar devices.

To complete the workshop with a non-parallel session, Olin Hartin of Freescale Semiconductor will greatly increase our understanding of "TCAD Simulation of Compound Semiconductor Electronic Devices". This workshop will begin with a review of the fundamentals of TCAD simulation and available tools. Then, there will also be a discussion of what to do prior to initiation of a simulation project and what to (and not to) expect. This will be followed by a brief overview of processing concepts as they relate to process simulation. There will then be a detailed discussion of process and device simulation of FETs and Bipolars. In this discussion, significant attention will be paid to calibration and what that really means. Finally, there will be some discussion of large signal simulation. Some special topics like design for manufacturing (DFM) may be discussed, time permitting.

Please see our website, www.csmantech.org for more information. The Workshop Registration fee covers all workshops. Except for student registration, the Workshop is *not* included in the Conference Registration Fee.

INDUSTRY EXHIBITS

During 2006, the compound semiconductor industry expanded at the most rapid pace since 2000. For much of the year, fabs were running at or near full capacity. While most of the revenue was generated by GaAs-related activity, GaN and SiC efforts grew rapidly. Equipment and material suppliers provide the infrastructure to make this activity possible. The conference Exhibition provides an opportunity for these suppliers to showcase their products and services.

The conference Exhibition starts on Monday evening, May 14, after the close of the Technical Workshops. It continues all day on Tuesday, May 15. The Exhibition provides an excellent forum for conference and exhibition attendees to interact in a relaxed forum. As with previous years, there will be three events held in the Exhibition area. Monday evening, the conference opens with the Exhibits Reception from 6:00pm to 9:00pm. On Tuesday, both a continental breakfast (7:00am – 8:00am) and the

Exhibition Luncheon (12:30pm – 1:35pm) will be held in the Exhibition area. Both Tuesday coffee breaks will also be held in the area, so there will be ample time for interaction with both current and potential customers.

For additional information, or to register for a booth, please visit our web site at www.csmantech.org, and click on the Exhibitors link. You can also contact the Exhibits Chair, Russ Kremer, at russ@fcm-us.com.

Exhibits Reception

The Exhibits Reception will be held in the Exhibits area Monday evening from 6:00pm – 9:00pm. Buffet style finger food will be available, so grab a plate and mingle with your colleagues and check out the exhibits. See what new products and services our vendors are offering.

Exhibits Luncheon

The Exhibits Luncheon will be held in the Exhibits area on Tuesday, from 12:30 p.m. – 1:35 p.m. While having your lunch, you can continue to interact with your vendors and colleagues from around the world.

Exhibitors' Forum

Again this year, we will offer vendors an opportunity to present their latest and greatest in a semi-formal presentation. Like last year's successful forum, we will have parallel sessions to allow more vendors to present. This year's forum will run on Tuesday from 1:35 p.m. – 3:30 p.m. Presentation slots are limited, so if you are interested in talking about your products, please sign up early. After the presentations, there will be an additional opportunity for conference attendees to ask questions and discuss your presentation further back at your booth during the afternoon coffee break.

INTERNATIONAL RECEPTION

MANTECH extends an invitation to family and friends that may be accompanying you at the Conference to join us at this special event Tuesday night. Guest tickets are $50 each. *We strongly encourage you to purchase guest tickets at the time of your registration to ensure space at the reception.*

CONFERENCE CLOSING RECEPTION

A Conference Closing Reception will wind up the 2007 edition of MANTECH. It will follow immediately after the Interactive Forum. Drinks and snacks will be provided to foster a congenial final opportunity to exchange business cards, ideas, and experiences.

Returning this year is a Feedback Form Raffle. Your opinion on the Feedback Form is very valuable to the MANTECH committees in structuring the conference and programs year-to-year and in choosing the best paper awards. This year, when you turn in your Feedback Form you enter a raffle. The prize is to be announced, but you know it will be fabulous! It's as simple as that. The drawing will be held at the Conference Closing Reception, though you need not be present to win. In addition, votes will be tallied and the Best Poster and Best Beautiful Picture Award winners announced.

At the time of this Advance Program preparation, a number of other exciting possibilities are being evaluated by the MANTECH committees for the Conference Closing Reception. Check our website for details!

2006 BEST PAPER AWARDS

CS MANTECH tradition is to formally recognize the authors of the best paper and best student paper of the previous conference, as determined from the conference attendee votes tallied from *your* feedback forms. These awards will be presented during the conference introductions on Tuesday, May 15.

The authors of the Best Paper receive the He Bong Kim award, named in honor of Dr. He Bong Kim, the founder of the International Conference on Compound Semiconductor MANufacturing TECHnology. The He Bong Kim award winners for the 2006 Conference are Toshihide Kikkawa, Kenji Imanishi, Masahito Kanamura, and Kazukiyo Joshin of Fujitsu Laboratories for their paper "*Recent Progress of Highly Reliable GaN-HEMT for Mass Production*."

The Best Student Paper for the 2006 Conference, "*Improvements in the Process for Electrodeposition of Au-Sn Alloys*," was authored by Nasim Morawej, Douglas G. Ivey of the University of Alberta, and Siamak Akhlaghi of Micralyne, Inc.. The principal student author, Nasim Morawej, will receive a special cash award of $1000.

Congratulations to both these award winning teams for their fine work!

SEMI STANDARDS MEETING

The SEMI Standards meeting is scheduled for Wednesday, May 16, from 7:30 p.m. to 9:00 p.m. (immediately following the Rump Sessions). The SEMI Compound Semiconductor (GaAs, InP and SiC) Committee invites MANTECH Conference attendees interested in the development of internationally approved standards for wafer specifications to attend this meeting. Topics being addressed are GaAs, InP, and SiC dimensions/orientations and electrical properties, epitaxial layer specifications (which properties should be specified, and how they are to be verified), and non-destructive test methods.

Based in San Jose, CA, SEMI is an international trade association serving more than 2,400 companies participating in the semiconductor and flat panel display equipment and materials markets. SEMI maintains offices in Brussels, Moscow, Tokyo, Seoul, Hsinchu, Beijing, Singapore, Austin, Boston and Washington, DC. For additional information, please contact: Co-Chair: James Oliver of Northrop Grumman at 410-765-0117 or *j.oliver@ngc.com*, Co-Chair: Russ Kremer of Freiberger Compound Materials at 937-291-2899 or *russ@fcm-us.com*, or SEMI Standards Engineer Ian McLeod at 408-943-6996 or *imcleod@semi.org*.

BEAUTIFUL PICTURE CONTEST

During the 2007 Conference we will be holding a "Beautiful Picture Contest", a variation on our traditional "Ugly Picture Contest." Have you discovered art during your work? A particularly striking micrograph of a defect? Beautiful crystalline structures? A particularly fine example of chip art? Find your pictures or images and enter them into our contest! The CS MANTECH community will be judging the images solely on their artistic content and presentation - there is no need to describe process details or to relate it to a manufacturing problem solved.

Celebrate art for art's sake! Please submit your art with a title by May 1, 2007 to contest chairs Drew Hanser and Miro Micovic at hanser@kymatech.com and mmicovic@hrl.com Fantastic prizes will be awarded to the submissions judged to be the most artistic. Share the art you have found working with compound semiconductors!

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TECHNICAL PROGRAM

Monday, May 14

WORKSHOP

Chair: Scott Sheppard, *Cree, Inc.*

8:00 AM **Welcome/Introductions**

8:15 AM **Surface and Thin Film Analysis for Compound Semiconductors**
Yumin Gao, *Evans Analytical Group*
OR
8:15 AM **High-Speed, Next-Generation Networks and the Role of the Semiconductor Industry**
Professor M. Kalam, *University of Texas at Dallas*

10:00 AM **BREAK**

10:15 AM **Space Qualification for Semiconductor Devices**
Sammy Kayali, *NASA Jet Propulsion Lab*
OR
10:15 AM **Application of MOS Technology to Silicon Carbide Devices**
Mrinal Das, *Cree, Inc.*

12:00 PM **WORKSHOP LUNCH**

1:15 PM **Intellectual Property: Know How and Why**
Harvey Kauget, *Phelps Dunbar, LLP*
OR
1:15 PM **Silicon Carbide Material, Processing and Device Historical Overview**
Professor Jim Cooper, Jr. and Mike Capano, *Purdue University*

3:00 PM **BREAK**

3:15 PM **TCAD Simulation of Compound Semiconductor Electronic Devices**
Olin Hartin, *Freescale Semiconductor*

5:00 PM **WORKSHOP CLOSE**

6:00 PM **EXHIBITS RECEPTION**

Tuesday, May 15

8:00 AM **Welcoming Ceremonies**
George Henry, *Northrop Grumman ES*
Conference Chair

8:10 AM **Conference Awards**
Chun-Lim Lau, *Booz Allen Hamilton*
Executive Advisor, Past Conference Chair

8:20 AM **Technical Program Highlights**
Marty Brophy, *TriQuint Semiconductor*
Publications and Technical Program Chair

SESSION 1: PLENARY
Chair: Marty Brophy, *TriQuint Semiconductor*

8:30 AM *Invited Presentation*
State of the Compound Semiconductor Industry: A Focus on Communications
Ralph Quinsey, *TriQuint Semiconductor*

9:00 AM *Invited Presentation*
GaAs Industry in Europe – Technologies, Trends and New Developments
Wolfgang Bösch, *Filtronic IP*

9:30 AM *Invited Presentation*
An Overview of EMCORE'S Multi-junction Solar Cell Technology and High Volume Manufacturing Capabilities
David Danzilio, *EMCORE Photovoltaics*

10:00 AM *Invited Presentation*
Bulk Acoustic Wave Devices – Why, How, and Where They are Going
Steven Mahon and Robert Aigner, *TriQuint Semiconductor*

10:30 AM **BREAK**

SESSION 2: BACKSIDE PROCESS I
Chair: Andrew Stoltz, *US Army, Night Vision Laboratory*

11:00 AM *Invited Presentation*
Process Considerations for Manufacturing 50 µm Thinned III-V Wafers
G. Cobb, H. Isom, C. Sellers, and V. Williams, *TriQuint Semiconductor*

11:30 AM **FFT (Flow Free Thin) Mold Study for 44mm Fine Pitch Device Application**
J.M. Liu, Y.S. Lu, and X.S. Pang, *Freescale Semiconductor, Inc.*

11:50 AM **High Temperature–Resistant Spin-On Adhesive for Temporary Wafer Mounting Using an Automated High-Throughput Tooling Solution**
A. Smith[1], W. Hong[1], R. Puligadda[1], T. Matthias[2], C. Brubaker[2], M. Wimplinger[2], and S. Pargfrieder[2], [1]*Brewer Science Inc.*, [2]*EV Group*

12:10 PM **Carrier Techniques for Thin Wafer Processing**
Karlheinz Bock, Christof Landesberger, and Sabine Scherbaum, *Fraunhofer-Institute*

12:30 PM **EXHIBITS LUNCHEON**

1:35 PM **Exhibitors' Forum**
Chair: Russ Kremer, *Freiberger Compound Materials U.S.A. Inc.*

3:30 PM **BREAK**

SESSION 3: RELIABILITY
Chair: Peter Ersland, *M/A-COM*

3:50 PM **Mechanisms of Premature HEMT Breakdown**
L. Gunter, W. Zhu, J. Hulse, J. Diaz, P. Seekell, W. Kong, K. Nichols, and P.C. Chao, *BAE Systems*

4:10 PM **The Role Of Substrate Dislocations In Causing Infant Failures In High Complexity InGaP/GaAs HBT ICs**
T.S. Low, K.W. Alt, R.E. Yeats, C.P. Hutchinson, D.K. Kuhn, M. Iwamoto, M.E. Adamski, R.L. Shimon, T.E. Shirley, M. Bonse, F.G. Kellert, and D.C. D'Avanzo, *Agilent Technologies, Inc*; A. Wibowo, S. Hassler, N. Pan, G. Hillier, *MicroLink Devices, Inc.;* H. Badawi, M. Young, W. Liu, *AXT, Inc.*

4:30 PM **On Wafer Reliability Test Bench for PHEMT and HBT Technologies**
F. Bourgeois, M. Lanz, G. Jonsson, H. Stieglauer, and D. Behammer, *United Monolithic Semiconductors*

4:50 PM **Study on Effect of Fabrication Process on TDDB Lifetime of MIM Capacitors**
T. Kagiyama, Y. Tosaka, R. Yamabi, and H. Yano, *Eudyna Devices Inc*

5:10 PM **Reliability of High-Speed Devices: Probing of Self-Heating with Nanosecond Time - Resolution**
M. Kuball, G.J. Riedel, J.W. Pomeroy, R. Simms, A. Sarua, *University of Bristol*: M.J. Uren, T. Martin, K.P. Hilton, J.O. Maclean, and D.J. Wallis, *QinetiQ Ltd.*

SESSION 4: DEVICES & MODELS
Chair: Patrick Fay, *University of Notre Dame*

3:50 PM **High-Efficiency and Low-Noise AlGaN/GaN HEMTs for K- and Ka-Band Applications**
Ming-Yih Kao, Cathy Lee, Paul Saunier, Hua-Quen Tserng, and Gary Christison, *TriQuint Semiconductor*

4:10 PM *Student Presentation*
A Temperature Dependent Scalable Large Signal InP/InGaAs DHBT Model
Mark Stuenkel, Yu -Ju Chuang, Kurt Cimino, and Milton Feng, *University of Illinois at Urbana-Champaign*

4:30 PM *Student Presentation*
HfO_2-based Metal-Oxide-Semiconductor Capacitors on n-InGaAs Substrate with a Thin Germanium Passivation Layer
Hyoung-Sub Kim[1], I. Ok[1], M. Zhang[1], F. Zhu[1], S. Park[1], J. Yum[1], S. Koveshnikov[2], W. Tsai[2], V. Tokranov[3], M. Yakimov[3], S. Oktyabrsky[3], and Jack C. Lee[1], [1]*The University of Texas at Austin,,* [2]*Intel Corporation, and* [3]*The University at Albany-SUNY.*

4:50 PM **Realization of InAlN/GaN Unstrained HEMTs on SiC Substrates with a 75 Å Barrier Layer**
G. H. Jessen, J. K. Gillespie, G. D. Via, A. Crespo, and D. Langley, *Air Force Research Laboratory*

5:10 PM *Student Presentation*
High Frequency Noise Characterization and Modeling of InGaP/GaAs SHBTs
Benjamin F. Chu-Kung, Kurt Cimino, Yu -Ju Chuang, Mark Stuenkel, and Milton Feng, *University of Illinois at Urbana-Champaign,* Glen Hillier and Noren Pan*, Microlink Devices*

7:00 PM **INTERNATIONAL RECEPTION**
(Buses start leaving at 6:30 PM)

Wednesday, May 16

SESSION 5: GaN RELIABILITY and TESTING
Chairs: Allen Hanson, *Nitronex Corporation*
David Via, *Air Force Research Lab*

8:00 AM *Invited Presentation*
Qualification and Reliability of a GaN Process Platform
S. Singhal, A.W. Hanson , A. Chaudhari, P. Rajagopal, T. Li, J.W. Johnson, W. Nagy, R. Therrien, C. Park, A.P. Edwards, E.L. Piner, I.C. Kizilyalli, and K.J. Linthicum, *Nitronex Corporation*

8:30 AM **Reliability Study of AlGaN/GaN HEMT Devices**
K. Matsushita, S. Teramoto, H. Sakurai, J. Shim, K. Takagi, H. Kawasaki, Y. Takada, and K. Tsuda, *Toshiba Corp.*.

8:50 AM **Trap Analysis of GaN-Insulated-gate-HEMT for High Reliability**
Toshihide Kikkawa, Masahito Kanamura, Toshihiro Ohki, Kenji Imanishi, Kozo Makiyama, Naoya Okamoto, Naoki Hara, and Kazukiyo Joshin, *Fujitsu Ltd. and Fujitsu Laboratories, Ltd.*

9:10 AM **Leakage Current Screening for AlGaN/GaN HEMT Mass-production**
F. Yamaki, K .Ishii, M. Nishi, H. Haematsu, Y. Tateno, and H. Kawata, *Eudyna Devices Inc.*

9:30 AM **Failure Mechanisms in GaN HFETs under Accelerated RF Stress**
A. Conway, M. Micovic, P. Hashimoto, M. Chen, and P. Willadsen, *HRL Labs*

SESSION 6: ETCH & CLEAN
Chair: Patrick Fowler, *Anadigics.*

8:10 AM **Improvement of Base Ideality Through Improved Surface Cleans**
Terry Daly, Jason Fender, Agni Mitra, Matthew Parker, Darrell Hill, and Adolfo Reyes, *Freescale Semiconductor, Inc.*

8:30 AM **Surface Preparation Study in GaAs HBT Process**
Yelda Recsei, Shiban Tiku, Catherine Luo, and Peter Zampardi, *Skyworks Solutions*

8:50 AM **Atomic Hydrogen Cleaning of Epi-ready InSb (100), (111)B, and GCIB Processed InSb (111)B Surfaces**
S.R. Vangala[1], H. Dauplaise[2], L.P. Allen[3], G. Dallas[3], C. Santeufemio[1], C. Lynch[2], K. Vaccaro[2], D. Bliss[2], and W.D. Goodhue[1], [1]*University of Massachusetts,* [2]*Air Force Research Lab, and* [3] *Galaxy Compound Semiconductors*

9:10 AM **A Comparison of High Density ICP and Low Density RIE Processing for HEMT Applications**
Rohit Khanna, Dave Johnson, and Russ Westerman, *Oerlikon USA,* Mike Clausen, Gayle Murdoch, Matthew O'Keefe, *Filtronic*, and Steve Pearton, *Univ. of Florida*

9:30 AM *Student Presentation*
High-density Plasma Etching of rf-Sputtered Indium-Zinc-Oxide Films in Ar, Ar/Cl and Ar/ CH_4/H_2 Chemistries
R. Khanna, W.T. Lim, L. Stafford, and S.J. Pearton, *University of Florida*, Jae-Soung Park, Ju-Il Song, Young-Woo Heo, Joon-Hyung Lee, and Jeong-Joo Kim, *Kyungpook National University*

9:50 AM **BREAK**

SESSION 7: NOVEL SUBSTRATES
Chairs: John Blevins, *AFRL*
Ruediger Schreiner, *AIXTRON AG*

10:20 AM **Vertical-HVPE as a Production Method for Free-Standing GaN-Substrates**
B. Schineller, J. Kaeppeler, and M. Heuken, *AIXTRON AG*

10:40 AM **Large Area Single Crystal Diamond Wafers; Applications, Status, and Future Perspective**
Patrick Doering, Alfred Genis, and Robert Linares, *Apollo Diamond, Inc.*

11:00 AM **GaN on SOD Substrates – The Next Step in Thermal Management**
Jerry W. Zimmer and Gerry Chandler, *Diamond Technologies Inc.*

11:20 AM **GaN-HEMT-on-Diamond Substrates for X-Band Applications**
Daniel Francis, Felix Ejeckam, John Wasserbauer, Firoz Faili, and Dubravko Babic, *Group4 Labs,* Petra Specht, Johnny Ho, and William Hong, *Department of Material Science and Engineering, U.C. Berkeley*

11:40 AM *Student Presentation*
AlGaN/GaN High Electron Mobility Transistors and Diodes Fabricated on Large Area Silicon on Poly-SiC (SopSiC) Substrates for Lower Cost and Higher Yield
T.J. Anderson[1], F. Ren[1], L. Voss[1], M. Hlad[1], B.P. Gila[1], S.J. Pearton[1], J.Kim[1], J. Lin[1], P. Bove[2], H. Lahreche[2], J. Thuret[2], and R. Langer[2], [1]*University of Florida,* [2]*PicoGiga International*

SESSION 8: BACKSIDE PROCESS II
Chair: Alex Smith, *Brewer Science, Inc.*

10:10 AM *Invited Presentation*
MMIC Packaging and Heterogeneous Integration Using Wafer-Scale Assembly
P. Chang-Chien, X. Zeng, K. Tornquist, M. Nishimoto, M. Battung, Y. Chung, J. M. Yang, Y. Yajima, C. Cheung, K. Luo, D. Eaves, J. Lee, J. Uyeda, and M. Barsky, *Northrop Grumman Space Technology*

10:40 AM *Student Presentation*
Development of Simple Electrolytes for the Electrodeposition and Electrophoretic Deposition of Pb-free, Sn-based Alloy Solder Films
Chunfen Han, Qi Liu, and Douglas G. Ivey, *University of Alberta*

11:00 AM **High Yield Intra-Cavity Interconnection Fabrication Method and Characterization Methodologies**
M. Yajima, P. Chang-Chien, X. Zeng, K. Luo, C. Cheung, K. Tornquist, and M. Barsky, *Northrop Grumman Space Technology*

11:20 AM **Development of a Solder Bumped RFIC Switch Process**
Suzanne Combe, Matthew O'Keefe, Robert Dry, and John Atherton, *Filtronic*

11:40 AM **Development of Backside Process for Alternative Die Attach on HBT**
Jason Fender, Terry Daly, Darrell Hill, Lakshmi Ramanathan, Phil Bowles, and Neil Tracht, *Freescale Semiconductor, Inc.*

12:00 noon **LUNCH (Attendees' Choice)**

SESSION 9: POWER TRANSISTORS
Chair: S.C. Shen, *Georgia Tech.*

1:00 PM **Influence of the Epitaxy on the Sub-threshold Drain Leakage Current and the Breakdown Voltage for GaAs pHEMTs**
P. Abele, F. Bourgeoise, J. Splettstoesser, and D. Behammer, *United Monolithic Semiconductors*

1:20 PM **Gain Enhancement of JP-HEMT Power Amplifier for Cellular Phone**
Kazuki Nomoto, Koichi Hirata, and Mitsuhiro Nakamura, *Sony Semiconductor Kyushu Corporation*

1:40 PM **High Voltage GaAs pHEMT Technology for S-band High Power Amplifiers**
David Fanning, Anthony Balistreri, Edward Beam, Kenneth Decker, Steve Evans, Robert Eye, Warren Gaiewski, Thomas Nagle, Paul Saunier, and Hua-Quen Tserng, *TriQuint Semiconductor*

2:00 PM **Development of High Breakdown Voltage InGaP/GaAs DHBTs**
Jiang Li, Cristian Cismaru, Pete Zampardi, Eugene Babcock, Mike Sun, and Ravi Ramanathan, *Skyworks Solutions* and Kevin Stevens, *Kopin Corporation*

2:20 PM **Industrial GaInP/GaAs high Power HBT Process for S-Band and L-Band Applications**
H. Blanck, G. Jonsson, L. Favede, G. Pataut, M. Bonnet, and D. Floriot, *United Monolithic Semiconductors*

SESSION 10: FRONTSIDE PROCESS
Chair: Karen Renaldo, *Northrop Grumman Corp.*

1:00 PM **0.10 µm Ion-Implanted GaAs MESFETs with Low Cost Process Production**
M. Watanabe, D. Fukushi, H. Yano, and S. Nakajima, *Eudyna Devices Inc*

1:20 PM **pHEMT Gate Formation Using a Dielectrically Defined Gate with No Plasma Damage**
Wayne Pickens, Brook D. Raymond, and John W. L. Dilley, *M/A-COM, Inc.*

1:40 PM **Planarization Process for Transparent Polyimide Coatings to Reduce Topography and Overburden Variation**
Wu-Sheng Shih[1], Jiro Yota[2], Ketan Itchhaporia[1], and Alex Smith[1], [1]*Brewer Science and* [2]*Skyworks Solutions*

2:00 PM **Low-Cost, High-Performance Multifunction X-band Control MMICs Using Ion-Implanted FET Technology**
M.J. Drinkwine, Hausila Singh, and Mike Ashman, *M/A-COM, Inc*

2:20 PM **Transfer Printed Heterogeneous Integrated Circuits**
Etienne Menard, Ralph G. Nuzzo, Joseph Carr, and John A. Rogers, *Semprius*

2:40 PM **BREAK**

SESSION 11: GaN & SiC POWER DEVICES
Chairs: Robert Sadler, *Northrop Grumman ES*,
Andy Souzis, *II-VI Inc*

3:10 PM *Invited Presentation*
High Voltage GaN-HEMTs for Power Electronics Applications and Those Current Collapse Phenomena under High Applied Voltage
Wataru Saito, Ichiro Omura, and Kunio Tsuda, *Toshiba Corporation*

3:40 PM **An 800W AlGaN/GaN HEMT for S-band High Power Application**
E. Mitani, M. Aojima, A. Maekawa, and S. Sano, *Eudyna Devices Inc.*

4:00 PM **Fabrication of Robust High-performance Floating Guard Ring Edge Termination for Power Silicon Carbide Vertical Junction Field Effect Transistors**
Victor Veliadis[1], Megan McCoy[1], Harold Hearne[1], Ty McNutt[1], Li-Shu Chen[1], Gregory DeSalvo[1], Chris Clarke[1], Bruce Geil[2], Dimos Katsis[2], and Skip Scozzie[2], [1]*Northrop Grumman STC and* [2]*Army Research Laboratory*

4:20 PM **Technological Challenges for Manufacturing Power Devices in SiC**
Peter Friedrichs, *SiCED GmbH.*

SESSION 12: III-V MOSFETs
Chair: Jon Abrokwah, *Freescale Semiconductor*

3:10 PM *Invited Presentation*
III-V MOSFETs With Native Oxide Gate Dielectrics – Progress and Promise
P. Fay, X. Li, Y. Cao, J. Zhang, T. H. Kosel, and D. C. Hall, *University of Notre Dame, Dept. of Electrical Engineering*

3:40 PM *Invited Presentation*
Enhancement-mode III-V MOSFETs with High-? Gate Dielectrics
Yanning Sun, E. W. Kiewra, S. J. Koester, J. P. de Souza, N. Ruiz, A. Callegari, K. E. Fogel, D. K. Sadana, J. Fompeyrine, D. J. Webb, J.P. Locquet, M. Sousa, and R. Germann, *IBM*

4:10 PM *Invited Presentation*
High Mobility III-V MOSFET Technology
M. Passlack, R. Droopad, K. Rajagopalan, J. Abrokwah, and P. Zurcher, *Freescale Semiconductor, Inc.*

6:30 PM – 7:30 PM
RUMP SESSIONS
Chair: Heather Knoedler, *Skyworks Solutions, Inc.*

1 **Do we really need photoresist? And, other fun cost savings ideas.**
Moderator: Pat Fowler, *Anadigics*

2 **IC Torture – How much torture testing do you need for a cell phone that's going to be thrown away in 18 months, if it lasts that long?**
Moderator: Peter Ersland, *M/A-Com*

3 **The best substrate for GaN Devices – Which one will come out on the bottom?**
Moderator: Al Hanson, *Nitronex*

4 **Oracle of Apollo – Solar cells, the next Olympian application**
Moderator: Steve Mahon, *TriQuint*

5 **Power Devices – Which will win?**
Moderator: Yohei Otoki, *Hitachi-Cable*

6 **BiFET over E/D PHEMT – Where's the beef?**
Moderator: Mike Sun, *Skyworks Solutions*

Thursday, May 17

SESSION 13: BiFET Technology
Chair: Paul Cooke, *IQE RF*

8:00 AM *Invited Presentation*
InGaP Plus ™: Advanced GaAs BiFET Technology and Applications
William Peatman, Mohsen Shokrani, Boris Gedzberg, Wojciech Krystek, and Michael Trippe*, ANADIGICS Inc.*

8:30 AM *Invited Presentation*
High-Performance BiHEMT HBT / E-D pHEMT Integration
T. Henderson, J. Middleton, J. Mahoney, S. Varma, T. Rivers, C. Nevers, and B. Avrit, *TriQuint Semiconductor*

9:00 AM *Invited Presentation*
Monolithic Integration of E/D-mode pHEMT and InGaP HBT Technology on 150-mm GaAs Wafers
Cheng-Kuo Lin, Tsung-Chi Tasi, Chih-Chuan Chang, Yi-Te Cho, Jian-Cheng Yuan, Chuan-Pin Ho, Tung-Yao Chou, Jen-Hao Huang, and Yu -Chi Wang, *WIN Semiconductors Corp.*

9:30 AM *Invited Presentation*
Commercial Viability of BiFET Technology for GaAs Power Amplifiers
Ravi Ramanathan, Mike Sun, Peter Zampardi, Andre Metzger, Vincent Ho, Peter Tran, Nick Cheng, Cristian Cismaru, Jiang Li, and Mark Kuhlman, *Skyworks Solutions*

10:00 AM **BREAK**

SESSION 14: MANUFACTURING AND YIELD
Chair: Steve Mahon, *TriQuint Semiconductor*

10:30 AM **Development and Ramping of pHEMT in an "HBT Fab"**
Mike Fresina, C. Barratt, W. Wohlmuth, R. Yanka, C. Santana, D. Pfabe, and C. Duncan, *RF Micro Devices*

10:50 AM **Computer Integrated Manufacturing (CIM) in Smaller GaAs Fabs**
Troy Sterk, Chris Denton, and Nick Naul, *TriQuint Semiconductor*

11:10 AM **Resist Dispense Volume Reduction Using the Six Sigma Methodology**
J. Riege, A. Canlas, D. Barone, D. Crawford, Y. Recsei, S. Mony, and N. Ebrahimi, *Skyworks Solutions*

11:30 AM **Realizing Throughput Improvement Through Machine Rate Modeling - A Case Study**
Sathish Mudabagila-Gowda, Marino F. Arturo, and Ariel Meyuhas, *MAX I.E.G*

11:50 AM **Gate Shorts: A Process Engineer's Nightmare**
Thorsten Saeger, Travis A Abshere, Fabian Radulescu, and Jack Lail, *TriQuint Semiconductor*

12:10 PM **INTERACTIVE FORUM LUNCH**

1:10 PM - 3:10 PM
SESSION 15: INTERACTIVE FORUM
Chairs: Michelle Bourke, *Surface Technology Systems*
Victoria Williams, *TriQuint Semiconductor*

15.1 **Studying Package Delamination by TOF-SIMS and XPS**
Luo JunHua, Yao JingZhong, Xu XueSong, and Adhihetty Indira, *Freescale Semiconductor*

15.2 **High-Volume Low Frequency Noise Characterization Technique**
Cristian Cismaru, Mark Banbrook, and Peter J. Zampardi, *Skyworks Solutions*

15.3 **Hydrogen Incorporation of Metal Gate HfO_2 MOS Structures on $In_{0.2}Ga_{0.8}As$ Substrate with Si Interface Passivation Layer**

InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, S. Koveshnikov[1], W. Tsai[1], V. Tokranov[2], M. Yakimov[2], S. Oktyabrsky[2], and Jack C. Lee, *University of Texas at Austin,* [1]*Intel Corporation,* [2]*University at Albany-SUNY*

15.4 **Uniformity Correlation of AlGaN/GaN HEMTs Grown on 3-inch SiC Substrates**
C. Lee[1], J. Jimenez[1], U. Chowdhury[1], M. Kao[1], P. Saunier[1], T. Balistreri[1], A. Souzis[2], and S. Guo[3], *TriQuint Semiconductor*[1]*, II-VI*[2]*, IQE RF*[3]

15.5 **Status of SEMI Standardization Efforts in Compound Semiconductors**
James D. Oliver[1] and Russ Kremer[2], *Northrop* [1]*Grumman ES,* [2]*Freiberger USA*

15.6 *Student Presentation*
Plasma Surface Pretreatment Effects on Silicon Nitride Passivation of AlGaN/GaN HEMTs
David J. Meyer, Joseph R. Flemish, and Joan M. Redwing, *Pennsylvania State University*

15.7 **Yield Enhancement of 0.15 µm pHEMT Millimeter Wave Power Amplifiers using an Effective Statistical Analytical Approach**
Nelson Chen, Scotie Lin, CK Lin, Wen Chu, Paul Yeh, Hank Chou, Joe Liu, and CS Wu, *WIN Semiconductors Corp.*

15.8 **Enhancement-mode Metamorphic nAlAs/InGaAs HEMTs on GaAs Substrates with Reduced Leakage Current by CF_4 Plasma Treatment**
Haiou LI, Chak-wah TANG, Kei May LAU, and Kevin J. CHEN, *Hong Kong University of Science and Technology*

15.9 **A Novel Water-Washable Coating for Avoiding Contamination During Dry Laser Dicing Operations**
K.C. Su, H.H. Lu, S.H. Chen , J. Moore,[2] and C.D. Tsai,[3] Y.C. Chou,[3] W.J. Wu,[3] and G.Q. Wu[3], *Lee Chang Yung Chemical Industrial Corp.,* [2]*DAETEC, LLC,* [3]*OPTO Tech Corporation*

3:10 PM **CONFERENCE CLOSING RECEPTION**
Best Poster and Best Beautiful Picture Award Presentations
Feedback Form Raffle Drawing

3:40 PM **END OF CONFERENCE**
Have a safe trip. See you next year!

TECHNICAL SESSIONS

SESSION 1: Plenary
Chair: Marty Brophy, *TriQuint*

Fighting the day-to-day battles in our fabs and labs, we can miss the big picture of the state of our industry. The keynote presentation of the conference aims to remedy this. TriQuint CEO Ralph Quinsey summarizes where we are and where we are going. A trend away from commodity to higher value supply is seen to have begun in 2006, and promises to continue. The second talk, by Filtronics CTO Wolfgang Bösch, focuses on the European compound semiconductor business: technologies, trends, and new developments.

Solar cells are a flourishing area of the compound semiconductor world that has been infrequently covered in this conference lately. In our third presentation, EMCORE Photovoltaics' David Danzilio will review the technology and manufacturing of multi-junction solar cells for both satellite and terrestrial applications. To complete the opening session, Bulk Acoustic Wave (BAW) devices, seen ever more frequently in or alongside our modules in cellular handset applications, are explained by Steve Mahon of TriQuint. Understanding what those devices are and how they are used is important for anyone wishing to have a complete picture of one of our key applications.

SESSION 2: Backside Process I
Chair: Andy Stoltz, *U.S. Army Night Vision Lab.*

This session concentrates on the complex challenges of backside processing compound semiconductor materials. The first paper of the session is an invited paper that gives a broad overview of backside processes and their impact on manufacturing at TriQuint Semiconductor. Wafer mounting, backside metallization, thinning techniques, wafer demount, wafer dicing, and pick & place techniques are discussed. Next, Freescale Semiconductor China examines a novel bonding process called Flow Free Thin (FFT). FFT requires no pressure during the bonding processing and its advantages and disadvantages are presented.

A collaboration of Brewer Science, Inc. and EV Group follows concerning different types of adhesives for temporary wafer bonding. A variety of properties of these adhesives and how they can be used with automated tools in manufacturing are examined. The last paper in the session is from the Fraunhofer Institute. It discusses temporary bonding techniques like thermal release tapes, soluble glues, and electrostatic carriers. Properties such as

allowed temperature range, bonding & de-bonding mechanisms, and compatibilities with different manufacturing techniques are examined.

SESSION 3: Reliability
Chair: Peter Ersland, *Tyco Electronics*

Four of the five papers in this session are related to manufacturing concerns. Our first paper describes work performed at BAE Systems to understand breakdown failures in HEMT devices. The authors have identified causes for these failures and discuss process improvements that mitigate the yield-limiting effects of poor breakdown performance. From HEMTs we move to HBTs, where reliability questions related to material quality have been a persistent concern. In a collaborative study led by Agilent Technologies, a relationship has been quantified between dislocation density in GaAs substrates and the occurrence of early device failures (infant mortality). From tests of a novel MSI reliability structure, we see what may be the first clear evidence of what process engineers have long believed – "It's the material's fault!"

Next, a group from UMS describes a wafer-level test system and associated methodology aimed at reducing the time and cost required to assess the impact of process changes on active device reliability. Our fourth paper (from Eudyna) discusses capacitor lifetime as a function of surface cleans and nitride deposition techniques. Voltage Ramped Dielectric Breakdown (VRDB) tests showed little difference between the various processes, but their impact becomes clearer when the Time Dependent Dielectric Breakdown (TDDB) technique is used.

Finally, researchers from the University of Bristol describe a system capable of mapping transistor temperatures with unprecedented spatial (0.5 - 0.7 µm) and temporal (40 nsec) resolution. This allows a better understanding of device thermal behavior under pulsed operation.

SESSION 4: Devices & Models
Chair: Patrick Fay, *University of Notre Dame*

Advances in device performance as well as accurate device modeling are important topics in the continued evolution of the industry. This session features five papers highlighting advances in these areas.

The first paper describes TriQuint's development of 0.25 µm AlGaN/GaN HEMTs for both power and low-noise applications in K and Ka bands. Then, researchers from the University of Illinois present a new large-signal model for InP/InGaAs DHBTs. The third paper in the session is a

joint paper from the University of Texas, Intel, and the University of Albany-SUNY that examines the role of Ge passivation layers in HfO_2/InGaAs metal-oxide-semiconductor capacitors, with implications for III-V field-effect transistors. Next, a group from the Air Force Research Lab describes their development of InAlN/GaN unstrained HEMTs on SiC. We finish with more work from the University of Illinois, this time on the noise performance of InGaP/GaAs HBTs.

SESSION 5: GaN Reliability and Testing

Chairs: Allen Hanson, *Nitronex Corporation*
David Via, *Air Force Research Laboratory*

AlGaN/GaN HEMTS for high power, high voltage applications are currently the subject of intense research. It seems every week there is an announcement of some new world record in power or power density. However, long-term reliability and an understanding of the underlying failure modes are not so well documented.

This session opens with an invited talk from Nitronex on the qualification process for their first production platform along with accompanying reliability results. The next three talks describe novel testing procedures used to analyze degradation characteristics and failure modes. Toshiba will present findings from their analysis of mesa versus implant isolation and discuss the fundamental mechanisms responsible for observed current degradation. Fujitsu will describe how they used pulsed I-V characterization of their insulated gate GaN MIS-HEMTs to investigate trap related issues and observed threshold shift. Then, Eudyna will report on a screening process used for their mass production of AlGaN/GaN HEMTs correlating substrate defects with leakage current. HRL will deliver the final talk of the session describing the results of their first comprehensive three-temperature accelerated RF life test at 10 GHz along with a discussion of observed failure mechanisms.

SESSION 6: Etch and Clean

Chair: Pat Fowler, *Anadigics*

This session offers presentations from both Industry and Academia. We first hear how Freescale and Skyworks Solutions have used HBT diode characteristics to drive improvements in their surface cleans. We then switch gears to the *in-situ* cleaning approach used for epi growth on InSb substrates.

We finish the session with two papers on dry etching with attention on the consequent surface damage. The first deals with selective etching of HEMTs comparing high

density ICP to pulsed low density RIE. The final paper presents the surface characterization results of IZO etched films as a function of etch chemistries and etch conditions.

Come learn and enjoy!

Session 7: Novel Substrates

Chairs: John Blevins, *Air Force Research Laboratory*
Ruediger Schreiner, *Aixtron*

This session reviews the latest progress in substrate improvements related to mismatch and temperature conductivity for GaN-based structures, an obstacle and a challenge for the last few years.

For deposition of blue-laser layer structures, reducing substrate dislocation density suggests the use of GaN vs. sapphire or SiC, but that is a costly approach. AIXTRON provides an insight into the design of its novel vertical HVPE equipment for growth of GaN boules and shows results on achieved material parameters.

Apollo Diamond follows with an overview of state-of-the-art single crystal CVD insulating or p-type diamond technology, including prospects for large area diamond wafers. Then, sp3 Diamond Technology reviews heat management considerations related to high density and high power devices. Their technology establishes a heat-spreading top plate of thin Silicon on Diamond (SOD) on which the GaN-based active structure can be deposited. Continuing in diamonds, Group4labs and U.C. Berkeley describe a novel lift-off/re-deposit of a GaN FET from a conventional substrate to a polycrystalline CVD diamond substrate.

Finally, a multi-disciplinary group from the University of Florida collaborating with PicoGiga reviews growth of AlGaN/GaN HEMT structures on silicon on poly-SiC substrates, providing comparable thermal conductivity to SiC and reduced cost. Impressive data on RF and DC performance of HEMTs and RF-to-DC rectifiers is reported.

SESSION 8: Backside Process II

Chair: Alex Smith, *Brewer Science, Inc.*

Papers in this session address specific details in advanced backside processing and packaging. The first paper from Northrop Grumman Space Technology describes the development of a low temperature, hermetically sealed, high-yield, wafer-level packaging technology compatible with MMIC fabrication processes. The second paper from the University of Alberta illustrates the development of Sn-

based solders e.g. the Sn-0.7wt%Cu alloy and eutectic and near-eutectic SAC (Sn-Ag-Cu) alloys, as alternatives to lead-based solders.

A follow-up paper from Northrop Grumman Space Technology then describes a technology capable of producing high yield Intra-Cavity Interconnects (ICICs). These interconnections provide signal routing between circuits on adjacent surfaces in a sealed package. Next, Filtronic IP describes the development of a solder bump, flip-chip process for RFIC switches. The session concludes with work completed by Freescale on an alternative process for HBT die attachment.

SESSION 9: Power Transistors
Chair: Shyh-Chiang Shen, *Georgia Tech*

This session presents several new developments on GaAs-based power transistors. The influence of epitaxy on sub-threshold drain leakage current and breakdown voltage is reviewed by researchers from United Monolithic Semiconductors. A Sony Semiconductor Kyushu team reports on a very significant 3-dB gain enhancement with novel gate-drain recessed structures in a junction pseudomorphic HEMT technology for WCDMA PAs.

A GaAs pHEMT technology with a capability of delivering 2.1-W/mm power output density and 64 % PAE at 28 V is then presented by TriQuint for S-band HPA applications. Similarly, InGaP/GaAs HBT technologies also strive to offer higher power performance with new designs. Contributors from Skyworks and Kopin discuss the development of an InGaP/GaAs DHBT technology with BV_{CEO} up to 40 V and f_T of 40 GHz at J_C = 0.3 mA/µm^2. To close the session, the manufacturability of a United Monolithic Semiconductor GaInP/GaAs high power HBT process for S-band and L-band applications is addressed.

SESSION 10: Frontside Process
Chair: Karen Renaldo, *Northrop Grumman*

What would a fabrication session be without discussions on improved manufacturability, lower cost, process control, higher yields, and high levels of integration? How about a fabrication session that discusses novel processing solutions for MESFETs, PHEMTs, HBTs and T/R Modules? This is exactly what this session has to offer.

The first paper from Eudyna describes their low cost optical 0.1-µm gate GaAs MESFET process. The paper illustrates an improved flow for their Single Resist Dummy (SRD) gate process. Then, M/A-COM transitions to smaller gates and/or field plates for improved

manufacturability. They present their work on a dielectrically defined gate process without plasma damage for their PHEMT products. Next, Brewer Science and Skyworks Solutions report on a planarization process solution for reducing polyimide coating topography for GaAs HBT devices.

The final two papers describe higher levels of MMIC integration. M/A-COM describes a low cost, high performance multifunction control MMIC technology that utilizes their successful MSAG process for phased array applications. The last presentation by Semprius illustrates an innovative and viable process that combines broad classes of dissimilar materials into heterogeneously integrated (HGI) electronic systems. Their unique methodology produces integration of compound semiconductors (i.e.: MESFET, HEMT, and GaN) with standard Si CMOS technology for high performance HGI electronic systems on ridged or flexible substrates.

SESSION 11: GaN & SiC Power Devices

Chairs: Andy Souzis, *II-VI Inc.*
Robert Sadler, *Northrup Grumman*

A formidable obstacle to high-voltage operation of power-switching devices has been current collapse from electron trapping in high electric fields. To start this session, an invited talk by Toshiba describes an effective solution, using an optimized MIS gate and field plate structure to yield devices with 2-m$\Omega \cdot cm^2$ on-resistance and 380-V breakdown, a combination 10 times better than the silicon limit. A new world record for pulsed power output from a transistor at S-band is then reported by Eudyna, with more than 800 W over 2.9 - 3.3 GHz from an AlGaN/GaN HEMT. Intended for radar applications, the 4-chip transistor has total gate periphery of 36 mm and shows better than 50 % drain efficiency over the band.

A breakdown voltage of over 2000 V is demonstrated by Northrop Grumman and the Army Research Laboratory for a SiC power-switching transistor. To achieve breakdown at 93 % of the 4H-SiC limit, this vertical JFET device employs an optimized guard ring structure with a p+ implant. Finally, a perspective on manufacturing challenges for SiC power MOSFETs and VJFETs, including n- and p-type ion implantation and contact formation, is offered by SiCED Electronics.

SESSION 12: III-V MOSFETs

Chair: Jon Abrokwah, *Freescale Semiconductor*

Significant progress continues to be made in III-V MOSFET technology with high mobility channels, a topic

of considerable interest for possible future applications in high-speed VLSI electronics and for RF wireless amplification and switching. Three invited speakers discuss progress and promise.

First, Professor Patrick Fay of Notre Dame presents enhancement mode MOSFETs with native oxides of InAlP as gate dielectrics. Dr Fay describes the oxide properties, interface characteristics, and enhancement mode devices. In the second talk, Dr Yanning Sun of IBM describes the formation of long and short gate length buried channel and surface channel, enhancement mode devices with high-k dielectric gate insulators, and high mobility $In_{0.7}Ga_{0.3}As$ channels.

Finally, Dr Matthias Passlack of Freescale Semiconductor describes advances of GaAs MOSFET technology based on gadolinium gallium oxide high-k dielectrics. Very high mobility channels, over 12,000, and 6,000 $cm^2/V\text{-}s$, respectively, in InP and GaAs based MOSFETs were demonstrated. The talk reviews the current state of materials, high – k dielectrics, interface properties, implant free devices, and high performance enhancement-mode transistor results.

RUMP SESSIONS
Chair: Heather Knoedler, *Skyworks Solutions, Inc.*

Come one, come all to The Greatest Session On Earth! The always popular and entertaining rump sessions provide a forum to share your wildest thoughts and craziest opinions, while stealing your competitors' best ideas! (Or, is it while learning from other experts in the industry?) This year there will be six sessions to amuse and delight you:

1. Do we really need photoresist? And, other fun cost savings ideas.
   Pat Fowler, Anadigics
2. IC Torture - How much torture testing do you need for a cell phone that's going to be thrown away in 18 months, if it lasts that long?
   Peter Ersland, M/A-Com
3. The best substrate for GaN devices – Which one will come out on the bottom?
   Al Hanson, Nitronex
4. Oracle of Apollo – Solar cells, the next Olympian application
   Steve Mahon, TriQuint
5. Power Devices – Which will win?
   Yohei Otoki, Hitachi-Cable Ltd. Japan
6. BiFET over E/D PHEMT – Where's the beef?
   Mike Sun, Skyworks Solutions, Inc.

What's better than a three-ring circus? Why a six-ring rump session of course! So, choose a topic, grab a free beer and some snacks, and join us for an hour of fabulous fun. Come share your opinions, argue your points, or just learn something new so you can impress your boss when you get back to work.

SESSION 13: BiFET Technology
Chair: Paul Cooke, *IQE RF*

Integration of Bipolar and FET devices on the same die has become a topic of significant interest within the GaAs RFIC market. The BiFET concept is well known and established within the Si industry, but it has only recently emerged as a viable, manufacturable technology within the GaAs field. Current BiFET implementations employing HBT and either PHEMT or MESFET technologies have enabled efficient, cost-effective PA designs to be achieved that are well suited for advanced mobile applications. This session contains presentations from four leading GaAs fabs actively engaged in BiFET technology at both development and production levels. The talks will provide an opportunity to assess the advantages, limitations, and problems associated with implementing and sustaining a commercial BiFET approach.

Anadigics first reports on a Front End Module designed and implemented using their "InGaP-Plus" technology, a combination of InGaP HBT and PHEMT processes currently in volume production. TriQuint Semiconductor then discusses a more complex combination of InGaP HBT and E/D PHEMT that provides additional design flexibility and is focused on retaining the respective stand-alone device performances. Next, researchers from WIN Semiconductor similarly report a combination of InGaP HBT and E/D PHEMT and the steps that have been developed to produce functional circuits using the technology. The final paper, from Skyworks Solutions, compares and contrasts the various options for HBT and either PHEMT or MESFET integration and how the choice of epi structure, fabrication requirements, and device performance tradeoff for the overall manufacturability and ultimate cost of a BiFET technology.

SESSION 14: Manufacturing and Yield
Chair: Steve Mahon, *TriQuint*

Presentations in this session represent the latest efforts from the largest compound semiconductor fabs in the world. The topics cover a wide range including cost reduction, yield improvement, throughput enhancement, process diversification, and even environmental impact.

RFMD leads off describing a significant change in their fab focus, moving from being a dedicated HBT fab to also doing pHMETs. This is no trivial adventure. Then TriQuint describes automation techniques for smaller sized fabs and how to balance the cost and benefit. Next, Skyworks completes the big fab trifecta with a report on resist dispense volume reduction for photo chemicals. The paper shows very impressive use reductions that go directly to the bottom line and to the effect on the environment. Max I. E. G. next looks at machine model techniques for throughput improvement, critical in these times of very fast wafer ramps. A second TriQuint paper closes the session, looking at a traditional process engineering project of increasing yield by reducing sub-micron defects – in this case Gate-Ohmic shorts. This session is a definite no-miss on your CS MANTECH dance card.

SESSION 15: INTERACTIVE FORUM

Chairs: Michelle Bourke, *Surface Tech. Systems*
Victoria Williams, *TriQuint Semiconductor*

A primary goal of the MANTECH conference is to encourage open discussion and the free exchange of ideas among conference participants. An integral part of the conference since 1994, the Interactive Forum presents an opportunity for informal discussions and face-to-face meetings between authors and participants. During the forum, the authors of all presented papers are available to discuss their results in more detail and to answer questions. In addition, there are a number of papers available for review only during the Interactive Forum. This provides a time for conference participants to view and discuss these papers, as well.

Authors from Sessions 1 through 7 will be available during the first hour of the Interactive Forum, while authors from Sessions 8 through 14 will be available during the second hour of the session. Authors from the “interactive-only” session, Session 15, will be available for both hours. Drinks and refreshments will be provided. At the end of the session votes will be tallied and the Best Poster winner will be announced and awarded in the Conference Closing Reception. The 2007 International Conference on Compound Semiconductor Manufacturing Technology encourages all participants to attend the Interactive Forum, participate in the discussions, and enjoy the refreshments!

Special Thanks to our 2006 Exhibitors

Accent Optical Technologies
AIXTRON AG
AROTEC/Nikko Materials
Asahi Glass Co., Ltd.
Aviza Technology, Inc.
AXT
BMR Technology Corporation
BOC Edwards
Brewer Science
Centrotherm GmbH + Co. KG
Compound Semiconductor Magazine
CompoundSemi Online, Inc.
Corning Tropel Corporation
Cree, Inc.
Diamond Wire Technology
Disco Hi-Tec America
Doe & Ingalls of NC.
Emcore Corporation
Engis Corporation
EpiWorks
Evans Analytical Group
Freiberger Compound Materials
GE Advanced Materials
Gold Canyon Resources Inc.
Hitachi Cable, Ltd.
III-V's Review
II-VI Incorporated, Wide Bandgap Materials Group
Insaco, Inc.
Intelligent Epitaxy Technology Inc.
IQE Inc.
Johnson Matthey
KLA-Tencor
Kopin
LayTec
Lehighton Electronics, Inc.
MAX International Engineering Group
MBE Technology Pte. Ltd.
MicroChem Corp
Neosemitech

(continued on next page)

Special Thanks to our 2006 Exhibitors (continued)

NOVASiC

Optical Reference Systems, Ltd.

Picogiga International - A Soitec Group Company

Reedholm Instruments

Riber

Rubicon Technology, Inc.

SAES Pure Gas, Inc.

SAMCO International, Inc.

Spectrum Processing Equipment

Sumika Electronic Materials, Inc.

Sumitomo Electric Semiconductor Materials, Inc.

Surface Technology Systems plc

SVT Associates, Inc.

SYNOVA S.A.

TDI Inc.

TecHarmonic, Inc.

TECHNOS International, Inc.

Tegal Corporation

Unaxis Wafer Processing

Vacuum Engineering & Materials Co., Inc.

Veeco Instruments

Vistec Electron Beam GmbH

Visual Photonics Epitaxy Company

Wafer World Inc.

GENERAL INFORMATION

2007 International Conference on Compound
Semiconductor Manufacturing Technology
May 14 – May 17, 2007
Hilton Austin
500 East 4th Street
Austin, Texas 78701

REGISTRATION INFORMATION (US$)

	On or before Apr. 20	After Apr 20
Full Conference Registration	$525.00	$625.00
Student Conference Registration	$125.00	$125.00
Government Conference Registration	$525.00	$525.00
One-Day Conference Registration	$300.00	$300.00
**** New Low Price ****		
Workshop Registration	**$175.00**	**$275.00**
Government Workshop Registration	**$175.00**	**$175.00**

Payment of the full, student, or government conference registration fee includes one copy of the printed Conference Digest, one copy of the Conference Digest on CD, and admission to all sessions and the exhibits. It also includes the International Reception, Exhibits Reception, Exhibits Luncheon, Rump Session Reception, Interactive Forum Reception, continental breakfasts, and refreshment breaks. Additional copies of the Conference Digest may be purchased at $140.00 each. Additional copies of the Conference Digest on CD may be purchased for $50.00 each.

The one-day registration includes admission to all sessions for that day, admission to the Exhibits Hall, buffet breakfast, break refreshments, and lunch (note that there is no lunch served on Wednesday). The Rump Session Reception or Interactive Forum Luncheon Reception is included on Wednesday and Thursday, respectively. It also includes a printed Conference Digest and a Conference Digest on CD. The one-day registration does *not* include admission to the International Reception. The one-day option can be taken only once during the conference.

Payment of workshop registration includes one copy of the Workshop Digest, continental breakfast, Workshop Luncheon and break refreshments. Additional copies of the Workshop Notes may be purchased at $100.00.

Registrants may pay by check, money order, bank draft or credit card. Make checks payable in U.S. dollars drawn on a U.S bank to: “GaAs MANTECH, Inc.” Your name and address must appear on checks, money order or bank drafts. The only acceptable credit cards are Master Card,

VISA, and American Express. REGISTRATION FORMS SENT WITHOUT PAYMENT WILL NOT BE ACCEPTED. All refund requests must be received by Lucky Gold at the convention services office shown below by April 20 for a full refund less a $25 processing fee. **NO REFUNDS AFTER APRIL 20.**

For Advanced Conference Registration, complete the enclosed Registration Form at the end of this Advance Program and return with payment by April 20 to:

CS MANTECH Conference
c/o Lucky Gold Co.
4126 Crescent Drive
St. Louis, MO, USA 63129
Phone: (314) 894-0080
Fax: (314) 894-0450
Email: LLLCPA@aol.com

Or register for the conference online at our Web Site at:
www.csmantech.org

HOTEL RESERVATIONS

A block of rooms at the Hilton Austin has been reserved for CS MANTECH participants and their guests. The special CS MANTECH room rate is $154.00 for single or double occupancy. 15% in taxes will be added to these rates.

To make a hotel reservation, please register online through our website at:
www.csmantech.org

Or complete the Reservation Form (at the end of this program) and return it directly to:

Austin Hilton
Reservations Department
500 East 4th Street
Austin, Texas 78701

Or FAX the Reservation Form to the Hilton Austin Reservations Department at: 512-469 0078

Or Reservations can be made by calling toll free: 1-800-HILTONS within North America. Please be sure to mention you are a CS MANTECH attendee.

We ask you to please support CS MANTECH and to enjoy all of the conference activities by staying at our official 2007 location, the Hilton Austin. GaAs MANTECH, Inc. will be penalized if our room block is not filled.

<u>Hotel reservations must be received BEFORE Friday, April 20, 2007 to qualify for a room in the CS MANTECH room block.</u> ***If the room block fills prior to the cut off date, reservations will be accepted based on space and rate availability, so RESERVE EARLY!*** An advance deposit or credit card is required to hold your room.

Reservations received after FRIDAY, April 20, 2007 will be accepted on a space- and rate-availability basis.

CONFERENCE REGISTRATION & INFO CENTER

Conference registration will open at the Salon H Prefunction area on the Sixth Floor of the Hilton Austin on Sunday night and will be open Monday through Thursday during the following hours:

Day	Date	Hours
Sunday	May 13th	6:30 PM – 8:30 PM
Monday	May 14th	7:00 AM – 10:00 AM
		1:00 PM – 3:30 PM
		5:00 PM – 7:30 PM
Tuesday	May 15th	7:00 AM – 11:00 AM
		1:00 PM – 5:00 PM
Wednesday	May 16th	7:30 AM – 10:30 AM
		12:30 PM – 5:30 PM
Thursday	May 17th	7:30 AM – 9:30 PM

A Conference Attendee list will be available at the Information Center on Thursday, May 17th.

MESSAGE BOARD

A Conference Message Board will be maintained at the Registration & Information Center during registration hours. Please advise callers who wish to reach you during the day to ask the hotel operator to deliver a message to the CS MANTECH Conference Registration Desk. Please check the message board periodically.

SPEAKER PREPARATION ROOM

Meeting Room 415 on the Fourth floor has been reserved for speaker preparation. This room will be open from 7:00 AM to 5:00 PM on Monday through Thursday, May 14-17. The room will be set up with appropriate previewing equipment.

THE CONFERENCE HOTEL

Hilton Austin
500 East 4th Street
Austin, Texas 78701
Room Reservations: 1-800-HILTONS within North America
General Information: 512-482-8000
General Fax: 512-469 0078

The 2007 CS MANTECH Conference will be held at the Hilton Austin in Austin, Texas. Located in downtown Austin, it is directly across the street from the Austin Convention Center. The Hilton Austin is also one block from the Sixth Street entertainment area and a short stroll to the entertainment, shopping, and dining in the Warehouse Entertainment District and 2nd Street District. The Hilton Austin's downtown location is also convenient to many attractions such as the Capitol Building, Bob Bullock Texas Historical Museum, and the LBJ Presidential Library.

The Hilton Austin features 800 rooms, each equipped with a spacious work desk with two phones (each with 2 lines), voicemail, and a data port offering high-speed wireless internet service. A hospitality center in each room includes a mini-bar and coffeemaker. Iron/ironing board and hair dryer are also standard in all rooms. The business center in the hotel offers copying and faxing services, and you can connect to the business center's printer directly from your room. The concierge service is eager to assist you with your needs. At the Hilton Austin, food and beverage amenities and services include two restaurants, a coffee shop, a lobby bar and 24-hour room service.

The Hilton Austin's Tower health club and spa can provide personal trainers, and features a full assortment of exercise equipment. Spa services include massages, manicures, pedicures, facials, body wraps, and a variety of special treatments. A 48-foot outdoor heated lap pool and Jacuzzi® are also available.

For more detailed information on the Hilton Austin, visit
http://www.hilton.com
or click on the hotel link at *www.csmantech.org*.
For more information on Austin activities, visit
http://www.austincityguide.com or
http://www.austinmetro.com

TRANSPORTATION TO THE HOTEL

The Hilton Austin is easily reached in about 15 minutes from the Austin-Bergstrom Airport.

Taxi: Taxis are available at the airport. Taxi rates from the airport to the Hilton Austin are approximately $25.00.

Shuttle: An airport shuttle is available to and from the Austin-Bergstrom Airport. The rate to and from the Hilton Austin is $13.00 per person.

DRIVING DIRECTIONS

From Austin-Bergstrom Airport: Exit the airport and take Highway 71 west approximately 5.5 miles to I-35. Merge onto I-35 North and take exit 234C. Turn left at the first stop light (6th Street). Travel west on 6th street 4 blocks. Turn left onto Neches. The hotel is on the left on the corner of 5th & Neches.

FINANCIAL ASSISTANCE

MANTECH strongly encourages and supports participation from academic delegates. Students and University Professors seeking financial assistance should contact George Henry, the 2007 Conference Chair, by e-mail at sponsorships@csmantech.org.

2007
MANTECH
Registration Form

Register (use only 1 method)
Online at www.CSMANTECH.org
OR Either Fax OR Mail to:

GaAs MANTECH, Inc.
c/o Lucky Gold Co.
4126 Crescent Drive
St. Louis, MO 63129
Phone: (314) 894-0080
Fax: (314) 894-0450

Registration Fees: *Includes one printed copy and one CD of the Conference Digest, admission to all sessions, Exhibit Hall, International and Exhibits Receptions, Exhibit Luncheon, Rump Session Reception, Interactive Forum Reception, continental breakfasts and refreshment breaks. (All fees in US$.)* ***EXCEPT FOR STUDENTS, CONFERENCE REGISTRATION FEE DOES NOT INCLUDE WORKSHOP REGISTRATION FEE.***

Full Early Registration through April 20.......$525 $_______
Full Registration after April 20.....................$625 $_______
One Day Registration*..................................$300 $_______
Check one: *May 15* ____ or *May 16* ____ or *May 17* ____
Government Registration**...........................$525 $_______
Student Registration (includes Workshop)....$125 $_______
Additional Copies of Conference Digest-$140 each $_______
Additional CDs of Conference Digest-$50 each $_______
Additional Tuesday Night International
Reception Tickets #______............... $50 each $_______

2007 Workshop on May 14:
Includes one copy of the Workshop Notes, continental breakfast, Workshop Lunch, and break refreshments
Workshop Early Reg. through April 20.........$175 $_______
Workshop Reg. after April 20........................$275 $_______
Government Workshop Registration………..$175 $_______
Additional Copies of Workshop Notes-$100 each $_______

2006 Digest and Workshop Information*:**
2006 Conference Digests... #_____.......$140 each $_______
2006 Conference CD.......... #_____.......$ 50 each $_______
2006 Workshop Notes .... #_____.......$100 each $_______

Total $______

* One-Day Registration can be used only once during the Conference. It includes a copy of the Conference Digest and CD. It does not include admission to the International Reception.

** Must fax proof of government employment if registering after April 20. Not for contractors.

*** Visit www.csmantech.org to order Conference Digests, Workshop Notes, or Workshop Videos for prior years.

Early Conference/Workshop Registration Cutoff Date
April 20, 2007

Conference Registration Form Continued

Please indicate which special events you plan to attend:

- ❑ Exhibits Reception (Monday evening)
- ❑ Exhibits Luncheon (Tuesday lunch)
- ❑ Exhibitors' Forum (Tuesday afternoon)
- ❑ International Reception (Tuesday evening)
- ❑ Rump Sessions (Wednesday afternoon)
- ❑ Interactive Forum (Thursday afternoon)

Please TYPE or PRINT clearly:

Name:____

Badge Name:____

Company:____

Address:____

City: ___________________ State: ______ Zip: ___________

Country: _____________

Phone: _______________________ Fax:_________________

Email:____

Payment must accompany registration form. Registration forms sent without payment will not be accepted. Requests for refunds (less $25 processing fee) must be made to address on prior page by April 20. No refunds after April 20, 2007.

Payment: ❑ VISA ❑ MasterCard ❑ AMEX

Name on Card:___________________________

Card No:________________________________

Exp. Date:_______________________________

❑ Check (payable to "GaAs MANTECH, Inc.")

Signature:____

MANTECH Hotel Registration Form

Register (use only 1 method)
Online at www.CSMANTECH.org
OR Either Fax OR Mail
to:

Hilton Austin

500 East 4th Street
Austin, Texas 78701
Phone: 512-482-8000
Fax: 512-469-0078

Sunday, May 13 through Thursday, May 17, 2007

Please TYPE or PRINT all information clearly.

Name____

Organization/Company______________________________

Address____

City___________________ State_________ Zip___________

Country________________ Telephone( )______________

Arrival Date_____________ Arrival Time________________

Departure Date___________ Departure Time______________

Check-in time is 3:00 pm. Checkout time is 12:00 noon.

# of rooms _____________ # of guests _________________

Room rate is valid for up to 2 guests/room. Add $20 to room rate for each additional guest. There is no charge for children up to and including the age of 18 years who share with their parents. Maximum occupancy is 4 adults per room.

Hotel Group Rate Cutoff Date – April 20, 2007

Hotel Registration Form Continued

❑ Non Smoking ❑ Smoking

❑ Single (1 King-sized Bed) $154 + 15%

❑ Double (2 Double Beds) $154 + 15%

If your requested room and bedding type are not available, an alternate will be assigned.

Special Requests____

____

All reservations must be guaranteed with a credit card, or a cash advance. A deposit equal to one night's stay is required to hold each reservation. The deposit is refundable if notice is received at least forty-eight (48) hours prior to scheduled check-in. One night's room and tax will be charged if cancelled less than *48 hours* prior to arrival.

Type of card: ❑ American Express ❑ Visa

❑ Diners Club ❑ Discover ❑ MasterCard

Cardholder name____

Credit Card Number_____________________________________

Expiration date____

Signature____

Enclosed is a Check/Money Order for $______________________

Please make check payable to
Hilton Austin.

Hotel Group Rate Cutoff Date – April 20, 2007

THE HILTON AUSTIN

MEETING ROOM LAYOUT