New method to monitor the frequency-dispersion in InGaAs/AlGaAs PHEMTs

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Abstract
The frequency-dispersion of PHEMTs with buried gate structures has been evaluated using the drain current transient measurement. We have observed a trap with a time constant of 9.0 µsec as an origin for the frequency-dispersion, which is closely correlated with the device structure. In order to quantitatively characterize the frequency-dispersion of the PHEMTs, we have introduced a new parameter of ∆Vth, which can be defined as a difference of threshold voltages for the devices with and without the inner recess. Then, we demonstrate that the Vth is quite effective to evaluate the frequency dispersion and to predict the power degradation at high-frequency operation.

INTRODUCTION
The InGaAs/AlGaAs pseudomorphic HEMTs (PHEMTs) have demonstrated superior high-power performances in wide-range frequencies. One of the most important issues in PHEMTs is to suppress the frequency-dispersion of the device characteristic such as a gate-lag phenomenon, which could be related to the surface states in the ungated region beside the gate [1][2]. The frequency-dispersion causes power degradation of PHEMTs at high frequency, and might lead to a decrease in their performances for long-term operation. In order to evaluate the frequency-dispersion of the device, the pulsed I-V measurement has been used, in which the transient of the drain current following the pulsed gate bias can be observed. However, from a manufacturing point of view, a more simple method to use for in-process monitoring is desirable to check the device quality with respect to the frequency-dispersion. In this paper, we propose a new method to predict the frequency-dispersion of PHEMTs only by using a simple DC measurement.

EXPERIMENTAL
Figure 1 shows a cross-section of the double-recessed In0.2Ga0.8As / Al0.28Ga0.72As PHEMT with a buried gate structure used in this study, in which the inner recess region was completely covered by the T-shaped Au/Pt/Ti gate metal. Such a buried gate structure has been widely used for power PHEMTs or MESFETs to suppress a frequency-dispersion with high breakdown voltage [2][3]. The gate length defined by the inner recess width was 0.6 µm and the length for the top portion of the T-shaped gate was 1.0 µm. The outer recess widths were 0.25 µm and 0.65 µm for the source and the drain sides, respectively. The epitaxial layer structures were grown by MOCVD.

In order to systematically investigate a relationship between the device structure and the frequency-dispersion, the samples with different threshold voltages (Vth) and the 2DEG densities (Ns) were prepared by changing the Schottky and the doping layer thickness. The inner and the outer recess depths were also changed by controlling the wet-etching time for the undope GaAs layer. After the Au/Pt/Ti gate electrode was formed using electron-beam evaporation and lift-off processes, the SiN/SiO2 passivation films were deposited on the device region by PECVD (Plasma Enhanced Chemical Vapor Deposition) and LPCVD (Low-Pressure Chemical Vapor Deposition), respectively.

The frequency-dispersion for the device was characterized using the test configuration in fig. 2. The gate width of the device was 10 µm. After a pulsed gate bias was applied, a transient for the drain current was measured using a digitizing oscilloscope through a 100 ohm load. The pulse width and period for the gate bias were set to 100 msec and...
The drain current reaches to its steady state during each pulse because a time constant for the transient is sufficiently short compared with the pulse duration. The threshold voltages of the samples were in the range from -0.3 V to -1.0 V, and the pulsed gate bias of -4 V / +1 V was applied at a constant drain voltage of +3 V.

**MEASUREMENT OF DRAIN CURRENT TRANSIENT**

The square points in fig. 3 show a typical drain current transient after the pulsed gate bias was applied. By fitting the measured data using exponential decay curves, the drain current transient can be expressed as,

\[
I_{ds}(t) = I_{ds0} - \Delta I_{ds1} \times \exp(-t/\tau_1) - \Delta I_{ds2} \times \exp(-t/\tau_2)
\]  

(1)

where \(I_{ds0}\) is the drain current at steady state and the other terms show the time-dependent current components due to the traps affecting the drain current transient. The \(\tau\) and \(\Delta I_{ds}\) would be correlated with the time constant and the density for the traps. The solid line in fig.3 illustrates the calculated curve by Eq.(1). In this case, we can fit the measured data by two kinds of traps named trap1 with \(\tau_1\) of 1.0 msec and trap 2 with \(\tau_2\) of 9.0 \(\mu\)sec, as shown in fig. 3. Figures 4 and 5 show the dependence of \(\Delta I_{ds1}\) and \(\Delta I_{ds2}\) on the inner recessed depth and the 2DEG density, respectively. The 2DEG density was varied by the doping layer thickness.
The threshold voltages for the devices in figs. 4 and 5 were controlled to be same for each inner recessed depth by changing the etching depth of the outer recess. As shown in figs. 4 and 5, the \( \Delta I_{ds2} \) decreased as increasing the inner recessed depth and the 2DEG density, while the \( \Delta I_{ds1} \) doesn't show any changing. This result clearly shows that the origin of the trap1 was in bulk region such as epi-layer / substrate interface and was not affected by the device structure. Moreover, the influence of \( \Delta I_{ds1} \) on the drain current transient was negligibly small for our devices compared with \( \Delta I_{ds2} \). Therefore, we focused on the trap2 to clarify the relationship between the device structure and the frequency-dispersion phenomenon.

As shown in figs 4 and 5, \( \Delta I_{ds2} \) can be suppressed by increasing the inner recessed depth and 2DEG density. This result means that a carrier concentration under the ungated surface region should be designed to be sufficiently large compared with that under the gate region to suppress the frequency-dispersion of the PHEMTs.

**MONITORING METHOD OF FREQUENCY-DISPERSION**

In order to quantitatively characterize the frequency-dispersion, we have introduced a new parameter of \( \Delta V_{th} \), which was defined as a difference of threshold voltages between the PHEMTs with and without the inner recess. The \( \Delta V_{th} \) can be expressed as,

\[
\Delta V_{th} = V_{th1} - V_{th2}
\]

Figure 6 simply illustrates the concept of \( \Delta V_{th} \). The \( I_{ds} \) characteristics measured for the devices with and without the inner recess are shown in the figure by square and circle points, respectively. If we regard the ungated surface region besides the gate as a parasitic transistor connected with the intrinsic region in parallel, its \( I_{ds} \)-\( V_{gs} \) characteristic can be simulated by the device without the inner recess. In a steady state, the intrinsic device, that is a PHEMT with the inner recess, limits the drain current because the current capacity for the parasitic transistor is sufficiently larger than that for the intrinsic one in all the gate biases. However, the threshold voltage for the parasitic transistor could shift to positive at just after the gate pulse is applied due to a slower response of a trapped charge in the surface states at SiO\(_2\)/GaAs interface. The triangle points in fig. 6 show the drain current for the parasitic transistor just after the gate pulse is applied \( (t << \tau_2) \). In this case, the extrinsic transistor collapses the maximum drain current for the intrinsic transistor. Therefore, the drain current gradually increases after the gate pulse is applied because the threshold voltage for the extrinsic transistor returns to its steady state by emitting carriers trapped in surface states with the time constant of \( \tau_2 \). The magnitude of the change in the threshold voltage for the extrinsic transistor \( (V_{trap}) \) could be related to the surface state density. In order to suppress the frequency-dispersion of the drain current for the PHEMTs, the \( \Delta V_{th} \) should be sufficiently larger than \( V_{trap} \).

Figure 7 shows the dependence of \( \Delta I_{ds2} \) on \( \Delta V_{th} \) for various PHEMTs with different threshold voltages, 2DEG densities and inner recess depths. The \( \Delta I_{ds2} \) was normalized using \( I_{ds0} \) in the steady state. As shown in fig. 7, normalized \( \Delta I_{ds2} \) strongly depends on \( \Delta V_{th} \), which suggests that the frequency-dispersion of PHEMTs can be well characterized by using the \( \Delta V_{th} \). This method is also useful to predict the power degradation of PHEMTs in high frequency regions. Figure 8 shows the dependence of the output power \( (P_{out}) \) at 1 MHz on \( \Delta V_{th} \). The output power was measured using the PHEMT of 140 \( \mu \)m width at the input power and the drain voltage of 5 dBm and 3 V, respectively. In spite of almost the same DC characteristics of those devices such as \( I_{ds} \) and \( g_m \), the \( P_{out} \) strongly depends on \( \Delta V_{th} \).
It can be concluded that the new parameter of $\Delta V_{th}$ is very effective to characterize the frequency-dispersion of PHEMTs. Because $\Delta V_{th}$ can be obtained by a simple DC measurement, it is also useful to control the high-frequency device performance in production line. Of course, it must be noted that the $\Delta V_{th}$ should be optimized in terms of other device characteristics such as a breakdown voltage, which would also depend on $\Delta V_{th}$.

CONCLUSIONS

The frequency-dispersion of PHEMTs with buried-gate structures was evaluated using the drain current transient measurement. Then we found the trap2 with a time constant of 9.0 $\mu$s as a main origin for the frequency-dispersion, which was closely correlated with the device structure such as inner recessed depth and 2DEG density. In order to quantitatively evaluate the frequency-dispersion for the devices with various structures, we introduced a new parameter of $\Delta V_{th}$, which was defined as a difference of threshold voltages between the PHEMTs with and without the inner recess. It was found that the $\Delta V_{th}$ was quite effective to characterize the frequency-dispersion. In order to suppress the frequency-dispersion of the PHEMTs, the larger $\Delta V_{th}$ was required. The $\Delta V_{th}$ was also useful to predict the power compression of the device, because it could be obtained by a simple DC measurement.

REFERENCES