Investigation of stressing InP/InGaAs DHBTs under high current density


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Abstract

We report on an InP/InGaAs DHBT technology, allowing high-speed operation with $F_t=150$ GHz, $F_{\text{max}}=200$ GHz at current densities of $J_c=110$ kA/cm$^2$, while maintaining $BV_{ceo}>12$ V. Moreover, excellent device uniformity and reliability is demonstrated under high current density stress with Time-to-Failure (TTF) > 45 years at $T_{\text{junc}}=110^\circ$C with $\Delta(\beta/\beta_0)<20\%$ making this technology suitable for high-speed IC fabrication.

INTRODUCTION :

InP based heterojunction bipolar transistors (HBTs) are an attractive technology to be used in high-speed (>40Gb/s) class ICs, see for example [1,2]. Consequently, intensive efforts have been devoted to device fabrication for further improvement of $F_t$ and $F_{\text{max}}$. Much progress has been made to improve high-speed device performance. $F_t$'s as high as 340 GHz have been reported at current densities exceeding $J_c=800$ kA/cm$^2$ [3]. High $J_c$ and $F_t$ is achieved by decreasing the collector thickness, which in turn will decrease the on-state breakdown voltage $BV_{ceo}$.

For successful implementation in high speed IC's in addition to high $F_t$ and $F_{\text{max}}$, a useful DHBT technology also requires high breakdown voltage $BV_{ceo}$, and excellent device yield as well as uniformity.

Long-term reliability is a major concern for any technology to be commercially viable. To our knowledge there have been a few reports on device uniformity, degradation and reliability of these type of devices [4,5]. Reliability up to now is mostly done under much lower current density stress as compared to high current density needed for high speed device operation [3,5]. In this paper we will report on a highyield, high performance InP/InGaAs DHBT technology with excellent device uniformity and long-term device reliability at high current density stressing.

The InP/InGaAs DHBT’s were grown on a 2-inch diameter (100) oriented InP substrate using Metal-Organic Molecular Beam Epitaxy (MOMBE). The base layer thickness is 500Å and activated base doping concentration is as high as $5x10^{19}$ cm$^{-3}$. To ensure high breakdown voltages of upto 12 V, a wide band-gap InP collector is used.

![Figure 1 : Gummel plot of the fabricated DHBT’s with $A_e=1.2 \times 7 \, \mu$m$^2$ emitter.](image1)

![Figure 2 : Common-emitter I-V characteristics. On-state breakdown voltage $BV_{ceo}>12$ V.](image2)
DEVICE TECHNOLOGY:

Figs. 1 and 2 depict the common-emitter IV and Gummel plot of a typical $A_e=1.2 \times 7 \, \mu m^2$ device. From Fig 2 it can be seen that $BV_{ce}>12V$. The microwave performance was characterized by on-wafer S-parameter measurements from DC up to 50 GHz. Fig 3 shows the cut-off frequency $F_t$ and maximum oscillation frequency $F_{max}$ as a function of collector current density $J_c$ at $V_{ce}=1.5 \, V$. To examine device uniformity, 180 transistors ($A_e=1.6 \times 3.4 \, \mu m^2$) distributed evenly on a wafer have been measured (see Fig 4). The tight distribution of the collector current at $V_{bc}=0.8 \, V$ ($I_c=1.4 \, mA$, $\sigma=0.1 \, mA$) indicates good device uniformity with this technology is obtained [4]. Device chains of 1000 devices show device yield to be > 99.99%.

DEVICE DEGRADATION:

Device degradation was studied by monitoring the on-chip degradation of the common emitter current gain $\beta$ at different ambient temperatures $T_{amb}$ under bias conditions of $J_c=150 \, kA/cm^2$ and $V_{ce}=1.5 \, V$ for $A_e=1.6 \times 3.4 \, \mu m^2$ devices. For improved device reliability carbon doping was used as the base dopant and the extrinsic emitter-base junction was passivated with an undoped latch layer. Fig 5 depicts the measured relative $\beta$ degradation as a function of stress time. To establish an activation energy, all degradation curves were converted back to $T_{amb}=80^\circ C$ so they match each other, assuming an Arrhenius type of function for the Temperature Acceleration Factor (TAF), see Fig 6.
Temperature Acceleration Factor (TAF) normalized at T\textsubscript{amb}=80°C.

Fig 7 displays the used TAF normalized at T\textsubscript{amb}=80°C versus inverse junction temperature T\textsubscript{junc}. An activation energy E\textsubscript{act} of 1.2 eV is derived from this figure. It should be noted that E\textsubscript{act} is determined over a large range of stress temperatures, as compared to [5], providing a check for low activation energy degradation and failures at low temperatures.

Figs. 8 and 9 show the influence of collector current density J\textsubscript{c} on the \(\beta\) degradation at a fixed ambient temperature of T\textsubscript{amb}=140°C. It can be observed from Fig 8 that \(\beta\) degradation increases considerably with increased current density (factor 4.5x is observed going from J\textsubscript{c}=145 to 190 kA/cm\textsuperscript{2}), resulting in a Current Acceleration Factor (CAF) of \(\eta=4\), see Fig 9. This indicates that the collector current density is an important parameter in determining the long-term device reliability of ultra-high speed InP HBTs operating at high collector current density’s J\textsubscript{c}.

The Gummel plot of a typical device before and after 1000 hrs stress at T\textsubscript{amb}=80°C is shown in Fig 10. It can be seen that \(\beta\) degradation is mainly due to an increase in base current, indicating that the decrease in common emitter current gain \(\beta\) is mainly caused by the degradation of the emitter-base junction.

This is confirmed by Fig 11, showing the Temperature Acceleration Factor (TAF) of \(\beta\) degradation for a device with and without the undoped base-emitter latch layer. Negligible shift in turn-on voltage V\textsubscript{be} is observed in Fig 10, which is most likely due to C-doped base used in our devices as compared to Be-doped InP HBT devices [5].
Temperature Acceleration Factor (TAF) [-]

Temperature Acceleration Factor (TAF) of a typical device with and without a undoped base-emitter latch layer.

FIGURE 11

DEVICE RELIABILITY:

For device reliability measurements 11 devices, distributed randomly across the wafer, were packaged and stressed at T_{amb}=140°C under high collector current density operation bias conditions for 1000 hrs. No burn-in was applied. Fig 12 displays the relative beta degradation as a function of stress time. It can be seen that the β degradation is uniform and no device failed after 1000 hrs. Also beta degradation is less than 20% (β/β_0 > 0.8). Based on an activation energy of E_{act}=1.2 eV derived earlier, this results in a Time-To-Failure > 45 years at T_{amb}=80°C/T_{junc}=110°C. This is sufficient for any advanced technology (typical product life of 15 years) to be utilized for high speed IC’s in optical communication systems.

CONCLUSIONS:

In summary, we investigated the long-term device reliability of our InP/InGaAs DHBT’s under high collector current stressing. Excellent device uniformity and reliability is demonstrated with Time-to-Failure (TTF) > 45 years and Δ(β/β_0) < 20% at T_{junc}=110 °C and \( J_c=110 \text{ kA/cm}^2 \). Furthermore, our InP/InGaAs DHBT technology, allows high-speed device operation with \( F_t=150 \text{ GHz} \), \( F_{max}=200 \text{ GHz} \) at current densities of \( J_c=110 \text{ kA/cm}^2 \), while maintaining \( \text{BV}_{ceo}>12 \text{ V} \).

REFERENCES:

[3] M. Ida et al., “InP/InGaAs DHBT with 341-GHz \( f_t \) at high current density of over 800 kA/cm\(^2\),” IEDM 2001, pp. 35.4.1-35.4.4.