Optimization of AlGaN/GaN HEMT Ohmic Contacts for Improved Surface Morphology with Low Contact Resistance

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Abstract
Good ohmic contacts with both low contact resistance and smooth surface morphology are required for the development of a robust manufacturing process of AlGaN/GaN based high power, high frequency MMICs. This extended abstract provides an optimization of the Ti/Al/Ni/Au ohmic metal stacks on AlGaN/GaN HEMT structures with a focus on the thickness of Ni and Au layer. It is found that the Ni thickness is the dominant factor to affect the contact resistance, while the Au thickness affects the surface morphology significantly. An optimal metal stack including a thick Ni and thin Au layer is found, which produces a low contact resistance around 0.26 ohm sq/mm and a smooth surface morphology with a surface roughness of 22nm. An excellent edge acuity is observed. Initial device results from optimized ohmic metal stack are also discussed.

INTRODUCTION
AlGaN/GaN HEMT devices offer high efficiency, ease of impedance-matching and broad bandwidth due to their attractive material properties. Therefore, these devices increasingly attract commercial and military interest for high power, high frequency RF power amplifier applications. The contact resistance of ohmic contacts affects the resistive heating, RF power output and power-added efficiency of the devices. Therefore, fabrication of low-resistance ohmic contacts to AlGaN/GaN HEMT structures is essential to achieve high performance devices. Ti/Al/Ni/Au has been widely used as ohmic contacts to AlGaN/GaN HEMTs since it produces a low contact resistance. This metallization, however, often exhibits a very bumpy surface morphology and a significant lateral overflow during alloying at high temperatures. The cause of the bumpy surface and lateral flow is likely due to the intermixing of Au and Al, which forms a viscous AlAu₄ phase at high annealing temperature [1, 2]. The overflow of ohmic metal can result in a short circuit between the source contact and gate metal, especially in short channel devices with a narrow gate-source spacing targeted for Q-band and higher frequencies. The device yield will be reduced significantly, especially for MMIC applications due to its high density device-integration and a fabrication process of several more metal layers. Furthermore, the poor surface morphology introduces challenges for chip-level visual inspection since the features of poor ohmic surface look similar to visual defects under the microscope. Therefore, it is necessary to have improved ohmic contacts on AlGaN/GaN HEMTs with both low contact resistance and smooth surface morphology.

Several groups presented an optimization of contact resistance for Ti/Al/Ni/Au metal stacks on AlGaN/GaN HEMTs. However, there is limited information about changes in the surface morphology of the metal stacks post-annealing [3, 4]. In this paper a detailed optimization of Ti/Al/Ni/Au metallization on AlGaN/GaN HEMT is presented with a focus on Ni and Au layer thickness. Contact resistance and surface morphology are studied as responses to the Ni and Au layer thickness with variations in RTA annealing temperature.

EXPERIMENTAL
AlGaN/GaN HEMT wafers used in this work were grown on 3” semi-insulating 6H-SiC substrates by MOCVD. The epi-structure consisted of an AlN nucleation layer, a GaN buffer and an Al₀.₂₄Ga₀.₇₆N barrier layer with a thickness of 180Å. The sample shows a sheet resistance of 450 ohm/sq, a sheet carrier concentration of 1×10⁹ cm⁻² and a mobility of 1400 cm²/vs.

The AlGaN/GaN HEMT device (T-gate with a gate length = 0.25μm) was fabricated by optical lithography except direct-write electron beam lithography for gate definition. Device isolation was done by multiple He damage implantations. Ti/Al/Ni/Au metal stacks with different Ni and Au thickness were used for ohmic contact. The thickness of Al and Ti were fixed with a ratio of 7.5. Two sets of samples were prepared with metal thickness listed in Table I, Set I with a thin Ni layer and Set II with a thick Ni layer. Shadow masks were used for the split of metal deposition. The samples were also annealed in a N₂ flowing ambient at various temperatures using rapid thermal annealing (RTA). Ni/Au was deposited as gate metal to the GaN HEMT devices. The distance of G-S and G-D is 1 and 1.5 μm, respectively.
Contact resistance of the ohmic contacts was measured by the transmission line method (TLM). The surface morphology was characterized using optical microscope, atomic force microscopy (AFM) and scanning electron microscopy (SEM) measurements. The root-mean-square (RMS) value for surface roughness of these metal contacts was measured from the analysis of a 10×10 μm² area on the ohmic metal pattern.

Table I Ohmic metal stacks with different Ni and Au thickness

<table>
<thead>
<tr>
<th>Sample</th>
<th>Ni layer thickness</th>
<th>Au layer thickness</th>
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<tbody>
<tr>
<td>Set I</td>
<td>Ni = 1X</td>
<td>Au = 1X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Au = 2.5X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Au = 5X</td>
</tr>
<tr>
<td>Set II</td>
<td>Ni = 2X</td>
<td>Au = 0.5X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Au = 2.5X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Au = 1X</td>
</tr>
</tbody>
</table>

RESULTS & DISCUSSIONS

Fig. 1 shows the surface morphology of post-annealed samples (Set I) with a thin Ni layer and different thickness of Au layer. It is clear that with a thin Ni layer (Ni = 1X), the sample with a thicker Au layer (Au = 5X) exhibits a very bumpy surface with the balling-up features after RTA. Decreasing Au thickness to 1X improves surface morphology significantly. It is widely reported that Ni would act as a diffusion barrier between the Au and the Al in the Ti/Al/Ni/Au metal stack to prevent the formation of a high resistive alloy called “purple plague” [1]. It is clear in our experiments that a thin Ni barrier (Ni = 1X) is effective to prevent the diffusion of Al and Au for the sample with a thin Au layer (Au = 1X). The thin Ni barrier (Ni = 1X), however, is not effective for the sample with a thicker Au layer (Au = 5X), where a poor surface morphology due to significant intermixing of Al and Au is observed.

Fig. 2 shows the contact resistance $R_c$ as a function of RTA temperature for the samples with thin Ni (Ni = 1X). The sample with a thick Au (Au = 5X) shows a low $R_c$ around 0.4 Ω•mm across a wide RTA annealing temperature window. Its surface morphology, however, is very poor shown in Fig. 1. It is also found in Fig. 2 that $R_c$ increases significantly from 0.4 to 1.2 Ω•mm with decreasing Au thickness from 5X to 1X. RTA annealing at different temperature doesn’t help much to lower $R_c$. Therefore, when a thin Ni (Ni = 1X) is used in Ti/Al/Ni/Au ohmic metal stack on AlGaN/GaN HEMT structures, it is necessary to increase Au thickness in order to have a low $R_c$ while sacrificing poor surface morphology. To solve this trade-off, Ni thickness was increased in our experiments.

Fig. 3 shows the contact resistance $R_c$ as a function of RTA temperature for the samples with a thick Ni (Ni = 2X). $R_c$ is constantly low around 0.2 ~ 0.4 Ω•mm for these samples, not sensitive to the changes of Au thickness. The process margins are also wide in terms of the changes of both RTA temp and Au thickness, which favors the manufacturing process of GaN HEMT MMICs with a low $R_c$.
always lower for the samples with a thick Ni (Ni = 2X) than those with a thin Ni (Ni = 1X) no matter the thickness of Au layer. Therefore Ni thickness is the dominant factor to affect the $R_c$ of Ti/Al/Ni/Au ohmic metal stack. A thick Ni (Ni = 2X) is preferred for achieving an ohmic metal contact with low contact resistance.

AFM was performed on those samples to check the surface roughness. Fig. 5 shows the comparison of RMS surface roughness among the two sets of samples annealed at 832°C for 30s. With increasing the Au layer thickness from 1X to 5X, the RMS value increases significantly from 20 to 150 nm no matter what the thickness of Ni layer is used. Therefore Au thickness is the dominant factor to affect the surface roughness of Ti/Al/Ni/Au metal stack. It is preferred to use a thin Au layer (Au = 1X) in order to maintain a flat surface of the ohmic metal after RTA annealing.

It is clear in Fig. 4 that $R_c$ decreases significantly from 1.2 to 0.26 ohm·mm with increasing Ni thickness for the samples with a thin Au layer (Au = 1X). In order to optimize the Ni thickness, several samples with different Ni thickness but same Au thickness (Au = 1X) were prepared. Fig. 6 show the contact resistance $R_c$ as a function of Ni thickness for the samples with a thin Au layer (Au = 1X) annealed at 832°C for 30s. With increasing Ni thickness from 1X to 1.75X, the $R_c$ drops significantly from 1 to 0.25 ohm·mm. There is a local minimum of $R_c$ around the Ni thickness of 1.75X. Jacobs et al. also reported a similar result that increasing or decreasing the Ni thickness degraded the contact resistance [1]. It is interesting that the $R_c$ decreased again in our experiments when Ni thickness over 2.5X. It is also observed that the surface morphology became rougher with increasing Ni thickness. With Ni layer thicker than 2.5X, the surface of ohmic metal became very dark. The sample likely became oxidized during RTA annealing although the annealing was performed under N$_2$ flowing ambient. This oxidation makes this very thick Ni layer not suitable for GaN HEMT technology in spite of the low $R_c$. Therefore, an optimal window of the metal thickness is around 1.8X for Ni and 1X for Au for achieving an ohmic contact with both low contact resistance and flat surface morphology.

Although the two samples (one with Au = 5X and Ni = 1X, another with Au = 1X and Ni = 2X) show similar $R_c$ around 0.3 ohm·mm in Fig. 4, their surface morphology is significantly different. The former shows a RMS value of 140 nm, while the other one only 22 nm. Fig. 7 show the SEM pictures of these two annealed Ti/Al/Ni/Au metal stacks. Their Al and Ti thickness were the same with a ratio of 7.5. The sample with a thin Ni (Ni = 1X) and a thick Au (Au = 5x) exhibits a very bumpy surface and significant lateral overflow with a surface roughness RMS of 150 nm. The other sample with a thick Ni (Ni =2X) and a thin Au (Au = 1X) shows a much smoother surface with a surface
roughness RMS of 22 nm. An excellent edge acuity with little lateral overflow is also observed after RTA annealing, as shown in Fig. 7. The mechanisms on how the two different ohmic metal stacks produced comparable low $R_c$ is under study by using scanning TEM.

![Fig. 7 SEM pictures of the Ti/Al/Ni/Au metal stack. RTA was done at 832°C for 30s.](image)

GaN HEMT devices with four gate fingers (each of 50µm width) and a total gate width of 200 µm were fabricated with the improved ohmic metal. The devices were tested on-wafer. Fig. 8 show I-V characteristics of a 200 um gate-periphery device, exhibiting an $I_{d_{\text{max}}}$ ~ 1020 mA/mm ($V_{gs}$ = 1V) and a peak transconductance $G_m$ of 370 mS/mm at $V_{ds}$ = 10V. The average $I_{d_{\text{max}}}$ at $V_{ds}$ = 10V and $V_{gs}$ = 1V across a 3” wafer is 960 mA/mm with a standard deviation of 30 mA/mm. The average peak $G_m$ and pinch-off voltage across a 3” wafer is 357 mS/mm and -3.5V with a standard deviation of 14 mS/mm and 0.06V, respectively. On-wafer small signal S-parameter measurement shows the average $f_c$ is 61.3GHz with a standard deviation of 1.3GHz across a 3” wafer with a bias of $V_{ds}$ = 10V.

![Fig. 8 I-V characteristics of a 200um gate-periphery device. (a) DC I-V curves, (b) Drain current ($I_d$) and transconductance ($G_m$) versus gate bias ($V_g$) with a drain bias of $V_{ds}$ = 10V.](image)

CONCLUSIONS

For Ti/Al/Ni/Au ohmic metal stack on AlGaN/GaN HEMT structures, the Ni thickness significantly affects contact resistance while the Au thickness dominantly affects surface morphology. Considering the requirement of both low contact resistance and smooth surface morphology for the ohmic metal, an optimal metal stack with a thick Ni ($Ni = 1.8X$) and a thin Au ($Au = 1X$) metal thickness ratio is found. This metal stack produces a low $R_c$ at 0.26 ohm•mm across 3” wafers and a broad RTA temperature window. The post-annealed metal surface also shows excellent edge acuity with a roughness value of 22 nm, which close to the surface roughness of the ohmic metal on GaAs pHEMT wafers. This optimized ohmic contact is very suitable for use in AlGaN/GaN HEMT MMICs with short gate-source/drain distances. The effects of this new metal stack on the device RF performance, wafer yield and device reliability are under further study.

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REFERENCES


ACRONYMS

HEMT: High Electron Mobility Transistor
MMIC: Microwave Monolithic Integrated Circuit
TLM: Transmission Line Method
RTA: Rapid Thermal Annealing
AFM: Atomic Force Microscopy
SEM: Scanning Electron Microscopy
RMS: Root Mean Square
STEM: Scanning Transmission Electron Microscopy