2010
International Conference on Compound Semiconductor Manufacturing Technology

May 17th - 20th, 2010

Register Online at
www.CSMANTECH.org

Portland Marriott Downtown Waterfront,
Portland, Oregon, U.S.A.

CONFERENCE AT A GLANCE

SUNDAY, May 16th

5:00 PM – 8:00 PM	**REGISTRATION** Ballroom Foyer

MONDAY, May 17th

7:00 AM – 7.00 PM	**REGISTRATION** Ballroom Foyer
7:00 AM – 8:30 AM	**Breakfast** Salon E
8:00 AM – 5:00 PM	**WORKSHOPS** Salons A - D
12:00 PM – 1:30 PM	**WORKSHOP LUNCHEON** Salon E
6:00 PM – 9:00 PM	**EXHIBITS RECEPTION** Exhibit Hall

TUESDAY, May 18th

7:00 AM – 11:00 AM 1:00 PM - 5:00 PM	**REGISTRATION** Ballroom Foyer
7:00 AM – 8:30 AM	**Continental Breakfast** Exhibit Hall
7:00 AM – 5:00 PM	**Internet Café** Exhibit Hall Foyer
8:00 AM – 8:30 AM	**OPENING CEREMONIES** Salons A - E
8:30 AM – 10:00 AM	**SESSION 1: Plenary I** Salons A - E
9:40 AM – 5:30 PM	**EXHIBITS OPEN** Exhibit Hall
9:40 AM – 10:20 AM	**BREAK** Exhibit Hall
10:20 AM – 11:50 AM	**SESSION 2: Plenary II** Salons A - E
11:50AM – 1:20 PM	**EXHIBITS LUNCH** Exhibit Hall
1:20 PM – 2:20 PM	**SESSION 3A: Plenary III** Salons A - E
2:20 PM – 2:40 PM	**BREAK** Exhibit Hall
2:40 PM - 3:40 PM	**SESSION 3B: ROCS Panel** Salons A - E
4:00 PM – 6:00 PM	**EXHIBITOR'S FORUM 1 - 3** Portland, Eugene, & Medford Rooms
4:00 PM – 6:00 PM	**STUDENT FORUM** Salem Room
6:30 PM – 10:30 PM	**INTERNATIONAL RECEPTION** Oregon Museum of Science & Industry 1945 SE Water Avenue

WEDNESDAY, May 19th

7:00 AM – 5:00 PM	**REGISTRATION** Ballroom Foyer
7:00 AM – 9:30 AM	**Continental Breakfast** Exhibit Hall
7:00 AM – 5:00 PM	**Internet Café** Exhibit Hall Foyer
7:00 AM – 11:00 AM	**EXHIBITS OPEN** Exhibit Hall
9:10 AM – 10:30 AM	**SESSION 4** Salon A - E
9:10 AM – 10:30 AM	**SESSION 5** Salon G - I
10:30 AM – 10:50 AM	**BREAK** Exhibit Hall
10:50 AM – 12:10 PM	**SESSION 6** Salon A - E
10:50 AM – 12:10 PM	**SESSION 7** Salon G - I
12:10 PM – 1:40 PM	**Lunch Break**
1:40 PM – 3:20 PM	**SESSION 8** Salon A - E
1:40 PM – 3:20 PM	**SESSION 9** Salon G - I
3:20 PM - 3:50 PM	**BREAK** Ballroom Foyer
3:50 PM - 5:30 PM	**SESSION 10** Salon A - E
3:50 PM - 5:30 PM	**SESSION 11** Salon G - I
5:30 PM – 7:00 PM	**RUMP SESSION RECEPTION** Ballroom Foyer
6:00 PM – 7:00 PM	**RUMP SESSIONS A-D** Portland, Eugene, Medford & Salem Rooms
7:00 PM – 9:00 PM	**SEMI Standards Meeting** Willamette Room (Lobby Level)

THURSDAY, May 20th

7:00 AM – 9:30 AM	**REGISTRATION** Ballroom Foyer
7:00 AM – 8:30 AM	**Continental Breakfast** Exhibit Hall Foyer
7:00 AM – 4:00 PM	**Internet Café** Gallery
8:00 AM – 9:40 AM	**SESSION 12** Salon A - E
9:40 AM - 10:00 AM	**BREAK** Ballroom Foyer
8:10 AM - 10:00 AM	**SESSION 13** Salon G - I

10:00 AM – 10:20 AM	**BREAK** Ballroom Foyer
10:00 AM – 11:40 AM	**SESSION 14** Salon A - E
10:20 AM - 11:50 AM	**SESSION 15** Salon G - I
11:50 AM – 1:20 PM	**25th Anniversary Luncheon** Exhibit Hall
1:20 PM – 2:50 PM	**SESSION 16** Salon A - E
1:20 PM – 2:50 PM	**SESSION 17** Salon G - I
3:00 PM – 4:30 PM	**INTERACTIVE FORUM** Salon F
4:30 PM - 5:00 PM	**CLOSING RECEPTION** Salon F

MESSAGE FROM THE CONFERENCE CHAIR

As we enter a new decade we are reminded of how far we have come as we proudly present the 25th Anniversary CS MANTECH Conference. Over the years we have traveled many ups and downs and 2009 was no exception. From the global economic despair at the beginning of the year to the generally positive outlook at the end, 2009 was truly a dramatic year. So, whether you started out holding "D" shaped wafers with tweezers back in the early days or you are new to the industry the CS ManTech Conference is the best place to check out what is new in the CS community.

This year we return to Portland, Oregon, the site of the second conference in 1987. The downtown Portland area offers a vast selection of dining and entertainment options. The Portland Marriott Waterfront is just steps away from the scenic Waterfront Park on the Willamette River and the RiverPlace Marina. Our International Reception will be held at the Oregon Museum of Science & Industry (OMSI) where we can tour the exhibits while enjoying the hospitality for which CS MANTECH is known.

CS MANTECH's mission is to foster communication between participants from academia, industry, and government. There will be a broad array of educational opportunities including our Monday workshops. Students can interact with potential employers. Industry veterans can keep contact with old friends, meet new ones, and take the pulse of the industry. The technical sessions will offer the current state of the art in material, processing, reliability and device technology across the compound

semiconductor spectrum. And you will not want to miss the special session on “Green CS Technology”.

New this year is the co-locating of the ROCS (Reliability of Compound Semiconductors) Workshop with CS MANTECH. Yes, the top CS Reliability event is occuring the same week as the top CS conference and top CS exhibition. The ROCS Workshop will be held in parallel to the CS MANTECH Workshops on Monday offering a new high water mark of learning opportunities.

This is the annual event where our industry comes together. Come join us.

Steve Mahon
TriQuint Semiconductor
Chairman, 2010 CS MANTECH Conference

2010 CONFERENCE SPONSORS

(Partial list, as of Feb 15th , 2010)

MANTECH is an independent not-for-profit organization whose mission is to promote technical discussion and scientific education in the compound semiconductor manufacturing industry. The continued success of the conference is enabled by donations from corporate sponsors. The 2010 CS MANTECH Conference Committee gratefully acknowledges the support from our sponsors.

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We would again like to thank our 2009 sponsors

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2010 CONFERENCE HIGHLIGHTS

The 2010 CS MANTECH program begins on Monday May 17th with a series of tutorial workshops. This year's workshops will focus on basic manufacturing technology of CS RF devices, from material to device process and will provide a broad overview of CS device manufacturing. In addition, this year CS MANTECH will host the internationally acclaimed ROCS Workshop (Reliability of Compound Semiconductors) which will be held on the opening day (Mon 5/17). The ROCS Workshop will present the latest results and new developments in all phases of Compound Semiconductor Reliability (see http://www.jedec.org/home/gaas/ for details).

On Monday evening the Exhibits opens at 6:00 pm with the traditional Exhibits Reception. The CS MANTECH exhibits are an excellent opportunity to view suppliers of materials, services and tools from around the globe. This is great time to renew old relationships and establish new ones while enjoying the fine food and libations of Portland.

The CS MANTECH Conference formally opens on Tuesday morning with a brief overview of the conference, and the awards presentation for the best papers from the 2009 conference. This is immediately followed by the two Plenary Sessions which will cover topics ranging from environmental issues in processing Compound

Semiconductors to new tunable passive device technology, to the latest in RF module technology.

After lunch in the Exhibits Hall, we'll see an analysis of our business and technology trends, and a Reliability panel session by ROCS task team. The Tuesday technical session will conclude with our Exhibitor's Forum. Also in parallel will be our Student Forum, which is designed to be an interactive session between students and the industry that is destined to hire them. As Tuesday evening approaches, we will move out of the Marriott to the Oregon Museum of Science, where we'll eat, drink and enjoy the river front view with old and new friends.

The Sessions on Wednesday morning start later, which allows additional opportunity to interact with the Exhibitors before the Exhibits close at noon. This morning will start our parallel sessions of world class technical papers and business insights of the compound semiconductor industry. One side of Wednesday's two parallel sessions focuses on emerging wide band-gap technologies, and the other on wafer fab management, processing and yield. These are topics for which CS MANTECH is well known.

Wednesday evening features the popular Rump Session. Eat, drink, and debate! Attendees may join any or all (if you move quickly) of the four parallel topics, where moderators will encourage informal, lively and highly interactive discussions.

Thursday morning continues with excellent technical papers on Emerging Technology including GaN Power Switching characteristics, process and packaging. We'll celebrate the 25th anniversary of MANTECH with a luncheon, in which the history of our unique conference will be presented. Thursday afternoon will include our closing two sessions and the Interactive Forum poster session. This poster session includes papers on a diverse range of topics, as well as poster versions of all the papers presented earlier in the technical program. Attendees will have the opportunity to meet with authors to discuss their papers in detail. Attendees of the Interactive Forum will vote for the best poster, and the winning author will receive the Best Poster Award.

The Conference Closing Reception will follow the Interactive Forum. In a warped and hopefully humorous variant of our historic "Ugly Picture Contest" as we did last year, we are holding an "Ugliest Process Tool Contest". Our closing reception will also feature a drawing for an iPod. All those who completed and submitted their Feedback Forms will have a chance to win!

WORKSHOPS

Each year in conjunction with the technical program, CS MANTECH offers Monday workshops on topics of interest to the compound semiconductor community. Past programs have offered tutorials on areas ranging from materials and processing, test and characterization, applications and market analysis, to engineering management and intellectual property rights. These invited talks by industry and academic leaders offer a forum for in-depth presentations and instruction.

This year's theme is an **Overview of Device Processing in III-V Manufacturing**. CS MANTECH is pleased to offer a day of talks on this subject that will provide a start-to-finish overview of processing steps for manufacturing wafers and devices for RF applications. The workshop will start with a high-level comprehensive overview followed by five talks that will explore different areas of the manufacturing process in detail. The planned tutorials will provide a good overview for those just wanting to learn more, but will also provide sufficient breadth of topics and detail that even those in the field will learn something new.

The workshops begin with a talk by Dr. Ravi Ramanathan from Skyworks Solutions, Inc. that provides a holistic overview of the III-V manufacturing process by taking us through a survey of the process flow, process integration, and testing steps used in device manufacturing. He will give a brief introduction to compound semiconductors and then discuss epitaxial materials and devices, general process flows, the role of technology development and manufacturing managers, and directions in which compound semiconductor manufacturing are headed. Dr. Ramanathan has a Ph.D. from the University of Poonta in India and he is the Director of Engineering at Skyworks Solutions Inc, leading the technology development group where he is involved in the development of devices and processes based on III-V compound/heterostructure semiconductors. In the second talk, Robert Yanka of RFMD will discuss the initial stages of the manufacturing process. His talk will focus on GaAs manufacturing from the production of substrates through characterization of finished epiwafers. Epitaxial growth techniques will be described along with in-situ and ex-situ characterization methods. The discussion will include a look into RFMD's MBE operation, covering organization, wafer management, process control and process improvement. Mr. Yanka has a M.S. in Physics from North Carolina State University and for the past ten years he has developed MBE growth processes for high volume manufacturing at RFMD, where he serves as the Manager of the MBE Development group.

The next two talks in the workshop focus on front-side processing of III-V device wafers. Dr. Shiban Tiku of Skyworks Solutions, Inc. will explore Front End of Line (FEOL) Device Processing, discussing figures of merit for different device structures, desired process and design characteristics, and the FEOL process flow, including a close examination of the critical process steps of etching, passivation, and pre-gate surface preparation. Dr. Tiku is the Manager of Yield and Process Integration at Skyworks and is responsible for Yield improvement of GaAs HBT devices in the areas of design, layout, wafer fabrication, back end processing and final packaged test. He has a Ph.D. in Materials Science from the University of Southern California. The fourth talk in the workshop will focus on the backend of front-side processing, with the speaker to be announced at the conference.

The last two talks will examine in detail the final stages of device processing. The fifth talk by Dr. Tim Whetten of Avago Technologies will explore the objectives and methods of processing the backside of wafers. A generalized process flow will be presented along with requirements of unit processes and methods of achieving those requirements, including dimensional control, materials interactions, assembly expectations and reliability issues. Several different process flows with different levels of complexity will be considered. Dr. Whetten received his Ph.D. in Materials Science from Cornell University. He is currently a senior Manufacturing Development Scientist in the Wireless Semiconductor Division of Avago Technologies developing and integrating new back-half GaAs manufacturing techniques. The final talk from Dr. Patty Chang-Chien of Northrop Grumman Aerospace Systems will discuss Wafer-Level Packaging and Wafer-Scale Assembly (WSA)Technologies. The talk will provide an overview of the wafer-level packaging and wafer-scale assembly technologies. The talk will briefly discuss motivation and benefits of these technologies as well as commonly used methods to accomplish packaging at the wafer level. Several demonstrations of this packaging technology, such as wafer-level packaged MMICs, and integrated RF front-end modules assembled by wafer-scale assembly, will be presented. Dr. Chang-Chien is the section manager of the WSA section in Semiconductor Products Department, Microelectronics Center at Northrop Grumman Aerospace Systems. She has a Ph.D. in Electrical Engineering from the University of Michigan.

INDUSTRY EXHIBITS

The CS MANTECH Exhibits are *the* annual venue for key CS suppliers and vendors to showcase their products and services. With the conference's technical focus on the "nuts and bolts" aspects of CS manufacturing, the CS MANTECH Exhibits represent an excellent opportunity for participating companies to meet and interact with the engineers, managers and key decision makers who shape and guide the industry. Exhibiting companies will gain excellent visibility to a wide range of CS focused participants from around the globe and be able to ensure their prominence and market position within the CS community.

The Exhibits will kick off on Monday evening with the Exhibits Reception. With food and drinks available, this will provide a great opportunity to catch up with friends, colleagues, suppliers, and even competitors on the first full evening of the conference. It represents an excellent networking opportunity and a window to meet and greet the assembling conference attendees who contribute to the continued success of the CS industry.

The Exhibits will kick off on Tuesday morning with a continental breakfast in the Exhibits Hall at 7.00 am. Following the Plenary Session, the Exhibits will open and be the location for the extended coffee breaks and our buffet style Exhibits Lunch

The popular Exhibitor's Forums will return and are scheduled for Tuesday afternoon. These allow participating companies to introduce new products or highlight company strengths in a short presentation. These forums are usually lively and typically provoke considerable interest from the conference attendees. The Exhibits will open again on Wednesday morning with a continental breakfast at 7.00am. The extended hours provide an ideal opportunity for both conference attendees and participating Exhibitors to follow up on interest generated by the forums, exchange business cards and finalize those last minute deals!

Those who know reserve their Exhibit space early! Visit our web site at www.csmantech.org, and click on the Exhibitors link for more details, including the sign up sheet and the link to the Exhibitors kit. Exhibitor Forum slots can also be reserved, but please note these are on a first come, first served basis and the number of slots is limited! For any questions related to Exhibiting at CS MANTECH,

please contact the 2010 Exhibits Chair, Paul Cooke, (732) 271 5990
email: exhibitor@gaasmantech.org

Special Thanks to our 2009 Exhibitors.

Kopin
EpiWorks
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Cree, Inc.
Wafer World Inc.
Hitachi Cable Ltd.
Bruker AXS, Inc.
KITEC/AxR Tech.
AIXTRON
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INTERNATIONAL RECEPTION

The 2010 CS MANTECH International Reception will be held at the Oregon Museum of Science and Industry (OMSI). OMSI is 219,000 square feet of brain-powered fun right across the Willamette River from the Marriott Hotel! Five enormous halls bring science to life with hundreds of interactive exhibits and displays. Dinner will be in the Turbine Hall which is home to many popular engineering and technological hands-on exhibits. In addition, you can experience their new *Space: A Journey to our Future* exhibit, as well as tour a real submarine. The USS Blueback (SS581) is one of the most modern U.S. submarines on public display anywhere in the country. She was the last fast-attack, diesel-powered sub built by the U.S. Navy. For those that wish to relax and enjoy some of Portland's finest wines there will be a local winery ("Hip Chicks do Wine") offering some wine tasting. MANTECH extends an invitation to family and friends that may be accompanying you at the Conference to join us at this special event Tuesday night. Guest tickets are $50 each. *We strongly encourage you to purchase guest tickets at the time of your registration to ensure space at the reception.*

2009 BEST PAPER AWARDS

CS MANTECH tradition is to formally recognize the authors of the best paper and best student paper of the previous conference, as determined from the conference attendee votes tallied from *your* feedback forms. These awards will be presented during the conference introductions on Tuesday, May 18th.

The conference Best Paper Award is named in honor of Dr. He Bong Kim, the founder of the International Conference on Compound Semiconductor MANufacturing TECHnology. The He Bong Kim award winner for the 2009 Conference is *Sarah Kurtz* of the *National Renewable Energy Laboratory* for **Opportunities for Development of a Mature Concentrating Photovoltaic Power Industry.**

The Best Student Paper voting for the 2009 Conference resulted in a co-award:

Lifetime Estimation of Intrinsic Silicon Nitride MIM Capacitors in a GaN MMIC Process

Sefa Demirtas[1], Jesus A. del Alamo[1], Donald A. Gajewski[2] and Allen Hanson[2]

[1]Massachusetts Institute of Technology, [2]Nitronex Corporation

Field Dependent Self-Heating Effects in High-Power AlGaN/GaN HEMT*M. Hosch[1], J. W. Pomeroy[2], A. Sarua[2], M. Kuball[2], H. Jung[3], and H. Schumacher[1]*
[1]Ulm University, Institute of Electron Devices and Circuits, [2]H.H. Wills Physics Laboratory, University of Bristol, [3]United Monolithic Semiconductors

The principal student authors will each receive a special cash award of $1000.

Congratulations to these award winning teams for their fine work!

SEMI STANDARDS MEETING

The SEMI Standards meeting is scheduled for Wednesday, May 19th, from 7:00 pm to 9:00 pm (immediately following the Rump Sessions) in the Willamette Room. The SEMI Compound Semiconductor (GaAs, InP and SiC) Committee invites CS MANTECH Conference attendees interested in the development of internationally approved standards for wafer specifications to attend this meeting. Topics being addressed are GaAs, InP, and SiC dimensions/orientations and electrical properties, epitaxial layer specifications (which properties should be specified, and how they are to be verified), and non-destructive test methods.

Based in San Jose, CA, SEMI is an international trade association serving more than 2,400 companies participating in the semiconductor and flat panel display equipment and materials markets. SEMI maintains offices in Brussels, Moscow, Tokyo, Seoul, Hsinchu, Beijing, Singapore, Austin, Boston and Washington, DC. For additional information, please contact: Co-Chair: James Oliver of Northrop Grumman at 410-765-0117 or *j.oliver@ngc.com*, Co-Chair: Russ Kremer of Freiberger Compound Materials at 937-291-2899 or *russ@fcm-us.com*, or SEMI Standards Engineer Ian McLeod at 408-943-6996 or *imcleod@semi.org*.

UGLIEST PROCESS TOOL COMPETITION

What old equipment is YOUR fab still using? We're having another of the MANTECH infamous photo contests and are seeking the oldest manufacturing equipment still being used in production!

We're soliciting photo entries of wafer manufacturing equipment that is used on a routine basis, as part of the regular manufacturing scheme. Sorry, but if it's sitting in a warehouse, it's ineligible. What do YOU have that qualifies?
Please submit a photo showing your antiquated equipment, along with appropriate identification (make, model, year, etc). A prize will be awarded based on attendee voting during the Interactive Forum. Your vender will LOVE this. Your Equipment Maintenance guys will be proud. And if you're really lucky, your boss will be SO embarrassed he'll fund a new acquisition to replace that piece of junk!! Contact Chris Youtsey for more information and to submit photos; cyoutsey@mldevices.com

CONFERENCE CLOSING RECEPTION

The Conference Closing Reception will bring to an end the 2010 edition of CS MANTECH. It will immediately follow the Interactive Forum. Drinks and snacks will be provided to foster a congenial final opportunity to exchange business cards, ideas, and experiences.

Returning this year is a Feedback Form Raffle. Your opinion on the Feedback Form is very valuable to the CS MANTECH committees in structuring the conference and programs year-to-year and in choosing the best paper awards. This year, when you turn in your Feedback Form you enter a raffle for an iPod Touch. It's as simple as that. The drawing will be held at the Conference Closing Reception, though you need not be present to win. In addition, votes will be tallied and the Best Poster presentation and Ugliest Process Tool Award winners will be announced.

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TECHNICAL PROGRAM
Monday, May 17th

WORKSHOPS

Chair*: Drew Hanser,SRI*

7:30 AM **Registration**

8:30 AM **Welcome and Introductions**

Workshop Session 1
8:45 AM **Process Flow, Process Integration, and Testing Overview**
Ravi Ramanathan, Skyworks Solutions

Workshop Session 2
9:45 AM **Substrates and Epitaxy in III-V Manufacturing**
Bob Yanka, RF Micro Devices

10:45 AM **BREAK**

Workshop Session 3
11:00 AM **Front End of Line (FEOL) Device Processing**
Shiban Tiku, Skyworks Solutions

12:00 PM **WORKSHOP LUNCHEON**

Workshop Session 4
1:00 PM **Device Processing in III-V Manufacturing: Front-Side Backend Processing**
Speaker TBD

Workshop Session 5
2:00 PM **Device Processing in III-V Manufacturing: Backside Wafer Processing**
Tim Whetten, Avago Technologies

3:00 PM **BREAK**

Workshop Session 6
3:15 PM **Wafer-Level Packaging and Wafer-Scale Assembly Technologies**
Patty Chang-Chien, Northrop Grumman Aerospace Systems

6:00 PM **EXHIBITS RECEPTION**

Tuesday, May18th

8:00 AM **Conference Opening**
Steve Mahon,TriQuint Semiconductor
Conference Chair

8:10 AM **2009 Conference Best Paper Awards**
Yohei Otoki, Hitachi Cable
Technical Program Chair

8:20 AM **Technical Program Highlights**
Yohei Otoki, Hitachi Cable
Technical Program Chair

SESSION 1: PLENARY I

Chair: Marty Brophy, *Avago Technologies*

8:30 AM *Invited Presentation*
1.1 Green Semiconductor Manufacturing - Potential New Routes Using Aqueous Solution Chemistry
David C. Johnson[1], Darren Johnson[1], John F. Wager[2] and Douglas Keszler[2]
[1]University of Oregon, [2]Oregon State University

9:00 AM *Invited Presentation*
1.2 Site Environmental Sustainability Achievements at Avago Technologies, Fort Collins, CO
Steve Wolley, Avago Technologies

9:30 AM *Invited Presentation*
1.3 Low Distortion Tunable RF Components, a Compound Semiconductor Opportunity
Cong Huang[1], Koen Buisman[1], Peter J. Zampardi[2], Lis K. Nanver[1], Lawrence E. Larson[3], and Leo C. N. de Vreede[1]
[1]Delft Institute of Microsystems and Nanoelectronics (DIMES), [2]Skyworks Solutions, and [3]University of California San Diego

10:00 AM **BREAK**

SESSION 2: PLENARY II - RF MODULES

Chair: Yohei Otoki, *Hitachi Cable* and Earl Lum, *EJL Wireless*

10:20 AM *Invited Presentation*
2.1 Market & Technology of RF Modules, Focusing on Front End Modules for Cellular Terminals
Y. Andoh, Navian, Inc.

10:50 AM **2.2 Panel Discussion**
Frank Juskey, TriQuint
Scott Klettke, Murata
Neal Mellen, TDK
Ray Parkhurst, Avago Technologies
Frank Stewart, RF Micro Devices
Peter J. Zampardi, Skyworks Solutions

11:50AM **EXHIBITS LUNCH**

SESSION 3a: BUSINESS ANALYSIS

Chair: Nick Kolarich, *Kopin Corporation*

1:20 PM *Invited Presentation*
3.1 Market Trends for Compound Semiconductor Enabled Devices, 2010 Update
Bruce A. Bernhardt, Research in Motion

1:50 PM *Invited Presentation*
3.2 The Evolution of the BTS Market: Going Green and Transitioning from a Hardware to Software/Services Oriented Business Model
Earl J. Lum, EJL Wireless

2:20 PM **BREAK**

SESSION 3b: TEAM TORTURE: DEVELOPING A STANDARD QUALIFICATION FOR POWER AMPLIFIER MODULES

Chair: Bill Roesch, *TriQuint Semiconductor*

2:40 PM **3.3 Panel Discussion**

4:00 PM: **EXHIBITORS FORUMS**

Please refer to the posted placards in the exhibit area for forum participants and scheduled presentations.

4:00 PM: **STUDENT FORUM**

6:30 PM: **INTERNATIONAL RECEPTION**

Wednesday May 19th

SESSION 4: DEVICE TECHNOLOGY

Chair: Kamal Alavi, *Raytheon, Corp.*

9:10 AM **4.1 Improvement in Yield and Power Drift for the Quater-Micron Optical Gate 8V Power pHEMT Technology**
Cheng-Guan Yuan and S M. Joseph Liu, WIN Semiconductor Corp.

9:30 AM **4.2 W-Band Penta-Composite Channel InAlAs/InGaAs Metamorphic HEMT for High Power Application and Comparison with Pseudomorphic HEMT**
Partha Mukhopadhyay[1], Sudip Kundu[1], Palash Das[1], Saptarshi Pathak[1], Edward Y. Chang[2], and Dhrubes Biswas[1]
[1]Indian Institute of Technology - Kharagpur, [2]National Chiao Tung University

9:50 AM **4.3 A Foundry-Ready Ultra High fT InP/InGaAs DHBT Technology**
Y. F. Yang, D. Rasbot, C. Chen, B. Lee, W. Yau, D. Hou, and D. Wang, Global Communication Semiconductors, Inc.

10:10 AM **4.4 The Development of 0.5um High Linearity and Good Thermal Stability AlGaAs/GaAs HFET for Wireless Infrastructure Application**
Cheng-Kuo Lin, Shu-Hsiao Tsai, Chao-Hong Chen, Ru-Yong Chen, Jen-Hao Huang, and Yu-Chi Wang, WIN Semiconductor Corp.

10:30 AM **BREAK**

SESSION 5: RELIABILITY

Chair**:** Peter Ersland, *M/A-Com Technology Solutions*

9:10 AM **5.1 High Volume Test Methodology for HBT Device Ruggedness Characterization**
Cristian Cismaru, Hai Banbrook, and Peter J. Zampardi. Skyworks Solutions

9:30 AM **5.2 TaN Resistor Reliability Studies**
Gergana I. Drandov and, Kenneth D. Decker, TriQuint Semiconductor

9:50 AM **5.3 Investigation and Improvement of Early MIM Capacitor Breakdown with a Focus on Edge Related Failures**
Jason Gurganus, Terry Alcorn, Andy MacKenzie, and Zoltan Ring, Cree, Inc.

10:10 AM **5.4 High Voltage Capacitors with Increased Lifetimes Using SiN Dielectrics**
Robert Slater, TriQuint Semiconductor

10:30 AM **BREAK**

SESSION 6: MANUFACTURING

Chair: Jim Crites, Cobham

10:50 AM **6.1 Skyworks Solutions Six Inch GaAs Conversion**
Glenn Hafer, Skyworks Solutions

11:10 AM **6.2 Automation for Better Fab Efficiency**
Nirav Thakker, Doug Beasley Alma Lopez, and Glenn Hafer, Skyworks Solutions

11:30 AM **6.3 Yield and Efficiency Improvements Using Multi-Field Hall Measurements for High Volume pHEMT Production**
Robert Yanka and Likang Li, RF Micro Devices

11:50 AM **6.4 Effective Manufacturing Utilizing Mass Metrology**
Sam Roadman[1], Liam Cunnane[2], Adrian Kiermasz[2], and Mark Berry[2]
[1]TriQuint Semiconductor, [2]Metryx, Ltd.

SESSION 7: GaN GROWTH AND CHARACTERIZATION

Chairs: Victoria Williams, Ruediger Schreiner, *AIXTRON AG*

10:50 AM *Student Presentation*
7.1 Comparative High-Temperature DC Characterization of HEMTs with GaN and AlGaN Channel Layers
M. Hatano[1], N.Kunishio[1], H. Chikaoka[1], J. Yamazaki[1], Z. B. Makhzani[1], N. Yafune[2,3], K. Sakuno[3], S. Hashimoto[4], K. Akita[4], Y. Yamamoto[4], and M. Kuzuhara[1]
[1]University of Fukui, [2]Japan Research and Development Center for Metal, [3]Sharp Corp., [4]Sumitomo Electric Industries, Ltd.

11:10 AM **7.2 Growth of LED Structures on Six Inch Sapphire: Challenges and Improvements**
R. Schreiner, A. Alam, H. Protzmann, B. Schineller, and M. Heuken, AIXTRON AG

11:30 AM **7.3 Benchmarking of Thermal Boundary Resistance of GaN-SiC Interfaces for AlGaN/GaN HEMTs: US, European and Japanese Suppliers**
Martin Kubal, Nicole Killat, Athikom Manoi, and James W. Pomeroy, University of Bristol

11:50 AM *Student Presentation*
7.4 Ultra-Low Contact Resistance for Self-Aligned HEMT Structures on N-Polar GaN HEMTs by MBE regrowth of InGaN-Based Contact Layers
Sansaptak Dasgupta, Nidhi, David F. Brown, Stacia Keller, F. Wu, T. Mates, James S. Speck, and Umesh Mishra, University of California, Santa Barbara,

SESSION 8: PROCESS METAL

Chair: Paul Werbaneth, *Tegal Corp*.

1:40 PM **8.1 Wafer Level Bump Technology for III-V MMIC Manufacturing**
X. Zeng, P. Chang-Chien, K. Hennig, C. Chueng, T. Chung, G. Akerling, J. Gan, J. Uyeda, M. Barsky, and A.Oki, Northrop Grumman Space Technology

2:00 PM **8.2 Development of an I-Line Negative Resist Process for High Resolution Liftoff Applications**
Suzanne Combe, Elda Clarke, and George Grama, TriQuint Semiconductor

2:20 PM **8.3 Challenges of Transferring a TaN Reactive Sputter Deposition Process from a Batch Tool to a Single Wafer Tool During a 4" to 6" Wafer Conversion**
Erika Schutte, Heather Knoedler, Ernesto Ambrocio, Skyworks Solutions

2:40 PM **8.4 Effects of Electron Radiation Generated During E-Beam Evaporation on a Photoresist Liftoff Process**
Kezia Cheng, Minh Le, Donald Mitchell, and Larry Hanes, Skyworks Solutions

3.00 PM **8.5 Improved Emitter Resistance Through the Use of Barrier Metals**
Alan Bratschun[1], Tao Yuan Shien
[1]Avago Technologies, [2]WIN Semiconductor

3:20 PM BREAK

SESSION 9: GaN DEVICES AND MANUFACTURING
Chair: Scott Sheppard, *Cree, Inc.*

1:40 PM **9.1 High Efficiency and Low Leakage AlGaN/GaN HEMTs for a Robust, Reproducible and Reliable X-Band MMIC Space Technology**
P. Waltereit, W. Bronner, R. Kiefer, R. Quay, J. Kuehn, F. van Raay, M. Dammann, S. Mueller, M. Mikulla, and O. Ambacher, Fraunhofer Institute - Freiburg

2:00 PM **9.2 Stable and Reproducible AlGaN/GaN HFET ProcessingHighly Tolerant for Epitaxial Quality Variations**
P.Kurpas[1], I. Selvanathan[1], M. Schulz[1], H.Sahin[2], P.Ivo[1], M. Matalla[1], J. Splettstoesser[2], A. Barnes[3], and J. Wuerfl[1]
[1]Ferdinand Braun Institut fuer Hoechstfrequenztechnik, [2]United Monolithic Semiconductors, [3]ESA/ESTEC

2:20 PM *Student Presentation*
9.3 Enhancement-Mode AlGaN/GaN HEMTs Fabricated by Standard Fluorine Ion Implantation
Hongwei Chen, Maojun Wang, and Kevin J. Chen, Hong Kong University of Science and Technology

2:40 PM **9.4 Optimization of AlGaN/GaN HEMTOhmic Contacts for Improved Surface Morphology with Low Contact Resistance**
H. P. Xin, S. Poust, W. Sutton, D. Li, D. Lam, I. Smorchkova, R. Sandhu, B. Heying, J. Uyeda, M. Barsky, M. Wojtowicz, and R. Lai, Northrop Grumman Space Technology

3:00 PM **9.5 Impact of Gate Metal Fringe Removal on Small Signal RF Gain of AlGaN/GaN HEMTs**
R. Behtash[1], J. R. Thorpe[1], S. Held[1], D. Schrade-Koehn[2], and H. Blanck[1]
[1]United Monolithic Semiconductors, [2]University of Ulm

3:20 PM BREAK

SESSION 10: PROCESS ETCHING
Chairs: Russ Westerman, *Plasma-Therm, LLC,* Chris Youtsey, *Microlink Devices*

3:50 PM **10.1 Elimination of Yield Loss Due to Rogue Polyimide Vias**
Yelda Rescei, Manjeet Singh, David Crawford, and Shiban Tiku, Skyworks Solutions

4:10 PM **10.2 The Use of Optical Emission Spectroscopy to Solve Mnufacturing Scaling Issues**
A. J. Stoltz, J. D. Benson, and P. J. Smith, U. S. Army RDECOM

4:30 PM **10.3 The Use of Optical Emission Interferometry (OEI) for Controlled Etching of III-V Materials**
D. Johnson and D. Geerpuram, Plasma-Therm, LLC

4:50 PM **10.4 Electrochemical Etching of Ion Implanted Channel Regions in GaAs**
J. Crites, J. Dilley, S. Kittinger, W. Pickens, M.Drinkwine, W. Polhamus, and M. Balzan, Cobham DES

5:10 PM **10.5 Pre-Photolithographic GaAs Surface Treatment for Improved Photoresist Adhesion During Wet Chemical Etching and Improved Wet Etch Profiles**
A. J. Grine[1], J. B. Clevenger[1], M. J. Martinez[1], F. H. Austin[2], P. S. Vigil[2], K. L. Romero[2], R. Timon[1], G. A. Patrizi[1], and C. T. Sullivan[1]
[1]Sandia National Laboratories, [2]LMATA

SESSION 11: EMERGING GaN-BASED BARRIER STRUCTURES
Chair: Dave Via, *Air Force Research Laboratory*

3:50 PM **11.1 Ultra-Thin Barrier Layers for mm Wave Frequencies in III-N HEMT Technologies**
J. K. Gillespie, A. Crespo, K. Chabak, Mauricio Kossler, V. Miller, M. Trejo, and G.D. Via, Sensors Directorate, Air Force Research Laboratory

4:10 PM *Student Presentation*
11.2 High Performance InAlN/GaN HEMTs on SiC Substrates
Han Wang, Jinwook W. Chung, and Tomas Palacios, Massachusetts Institute of Technology

4:30 PM *Student Presentation*
11.3 N-Face GaN-Based Microwave HEMTs by Plasma-Assisted MBE
Man Hoi Wong[1], Yi Pei[1], David Brown[1], James S. Speck[1], and Umesh K. Misha[1], Hyeongnam Kim[2], Michael L. Schuette[2], Venkatesh Balasubramanian[2], and Wu Lu[2]
[1]University of California, Santa Barbara, [2]The Ohio State University

4:50 PM *Student Presentation*
11.4 Source/Drain Regrowth in AlN/GaN High Electron Mobility Transistors
Chuanxin Lian, Yu Cao, Ronghua Wang, Guowang Li, Tom Zimmermann, Debdeep Jena, and Huili Grace Xing, University of Notre Dame

5:10 PM **11.5 Demonstration of Enhancement Mode AlN/Ultrathin AlGaN/GaN HEMTs using a Selective Wet Etch Approach**
T. J. Anderson[1], M. J. Tadjer[2], M. A. Mastro[1], J. K. Hite[1], K. D. Hobart[1], C. R. Eddy, Jr[1]., and F. J. Kub[1]
[1]Naval Research Laboratory, [2]Department of Electrical and Computer Engineering, University of Maryland

5:30 PM **RUMP SESSION RECEPTION**

6:00 PM **RUMP SESSIONS**

Chair: TBD

SESSION A: Looking at 25 Years: Best Moves and Biggest Flops
Moderator: Steve Mahon, TriQuint Semiconductor

SESSION B: When Does GaN Get Into Consumer Electronics?
Moderator: Ruediger Schreiner, AIXTRON AG

SESSION C: Decline of Western Civilization: Western v. Asian Fabs
Moderator: Joyce Ferrante, Marubeni America

SESSION D: **What I REALLY Think About My Competitor**
Moderator: Paul Cooke, IQE RF

7:00 PM **SEMI STANDARDS MEETING**

Thursday May 20th

SESSION 12: EMERGING TECHNOLOGY A

Chair: Amy Liu, *IQE Inc.*

8:00 AM *Invited Presentation*
12.1 Compound Semiconductor Based Tunnel Transistor Logic
Suman Datta, Pennsylvania State University

8:30 AM *Student Presentation*
12.2 Enhancement Mode Pseudomorphic $In_{0.22}Ga_{0.78}As$-Channel MOSFETs with InAlP Native Oxide Gate Dielectric
Xiu Xing and Patrick Fay, University of Notre Dame

8:50 AM *Student Presentation*
12.3 A Study on the Base Recombination Current in NPN GaN/InGaN DHBTs Using a Direct-Growth Technique
Yi-che Lee, Hee-Jin Kim, Suk Choi, Russell D. Dupuis, Jae-Hyun Ryou, and Shyh-Chiang Shen, Georgia Institute of Technology

9:10 AM *Invited Presentation*
12.4 Recent Progress in Rare Earth-Doped Semiconductors
Yasufumi Fujiwara, Atsushi Nishikawa, and Yoshikazu Terai, Osaka University

9:40 AM **BREAK**

SESSION 13: GaN POWER SWITCHING

Chair: George Henry, *Northrop Grumman ES*

8:10 AM *Invited Presentation*
13.1 GaN on Si-Based Power Devices: An Opportunity to Significantly Impact Global Energy Consumption
Michael Briere, ACOO Enterprises

8:40 AM **13.2 GaN-on-Si for Power Conversion**
M. Germain, S. Degroote, J. Derluyn, M. Van Hove, K. Cheng, M. Leys, J. Das, D. Visalli, D. Marcon, F. Medjdoub, K Geens, J. Viaene, B. Siimus, and G. Borghs, III-V Process Technology, IMEC

9:00 AM *Student Presentation*
13.3 AlGaN/GaN Schottky Barrier Diodes Employing Diamond-Like Carbon Passivation
Ogyun Seok[1], Young-Hwan Choi[1], Minki Kim[1], Jumi Kim[2], Byungyou Hong[2], and Min-Koo Han[1], [1]Seoul National University, [2]Sungkyunkwan University

9:20 AM *Student Presentation*
13.4 AlGaN/GaN Dual-Channel Lateral Field-Effect Rectifier with Punch-Through Breakdown Immunity and Low On-Resistance
Chunhua Zhou[1], Wanjun Chen[1], Edwin L. Piner[2], and Kevin J. Chen[1]
[1]Hong Kong University of Science and Technology, [2]Nitronex Corp.

9:40 AM *Student Presentation*
13.5 High Breakdown Voltage AlGaN/GaN HEMTs Employing Recessed Gate Edge Structure
Minki Kim, Young-Hwan Choi, Jiyong Lim, Young-Shil Kim, Ogyun Seok, and Min-Koo Han, Seoul National University

10.00 AM **BREAK**

SESSION 14: EMERGING TECHNOLOGY B
Chair: Andreas Eisenbach, *IQE plc*

10:00 AM *Invited Presentation*
14.1 Silicon Carbide Micro/Nano Systems for Extreme Environment
Roya Maboudian, University of California, Berkeley

10:30 AM *Invited Presentation*
14.2 Record Cell Efficiencies Hold Promising Future for Thin-Film Photovoltaics
Chris Constantine, Oerlikon Solar AG

11:00 AM *Student Presentation*
14.3 Design and Layout of Multi-GHz Operation of Light Emitting Diodes
Chao-Hsin Wu, Gabriel Walter, Han Wui Then, and Milton Feng, University of Illinois

11:20 AM *Student Presentation*
14.4 High Output Power Density and Low Leakage Current of InGaN/GaN Nanorod Light Emitting Diode with Mechanical Polishing Process
Liang-Yi Chen, Ying-Yuan Huang, Chun-Siang Chang, and Jian-Jang Huang, National Taiwan University

11:40 AM LUNCH BREAK
Open

SESSION 15: BACKSIDE PROCESSING
Chair: Michelle Bourke

10:20 AM *Invited Presentation*
15.1 Backside Process Considerations for Fabricating Millimeter-Wave GaN HEMT MMICs
Naoya Okamoto, Toshihiro Ohki, Kozo Makiyama, Atsushi Yamada, Satoshi Masuda, Masahito Kanamura, Yoichi Kamada, Kenji Imanishi, Hisao Shigematsu, Toshihide Kikkawa, Kazukiyo Joshin, and Naoki Hara, Fujitsu Ltd., and Fujitsu Laboratories, Ltd.

10:50 AM **15.2 Mobile Electrostatic Carrier (MEC) for a GaAs Wafer Backside Manufacturing Process**
H. Stieglauer[1], J. Noesser[1], A. Miller[1], G. Jonson[1], D. Behammer[1], C. Landesberger[2],H.-P. Spoehrle[2], and K. Bock[2]
[1]United Monolithic Semiconductors,
[2]Franuhofer Institute - Munich

11:10 AM **15.3 Low RF Power SiC Substrate Via Etch**
Ju-Ai Ruan, Sam Roadman, and Wade Skelton, TriQuint Semiconductors

11:30 AM **15.4 Stress Suppression of Backside Metal in GaAs Devices**
Koichiro Nishizawa, Katsuhisa Kitano, and Hirohumi Nakano, Mitsubishi Electric Co.

11:50 AM LUNCH BREAK

SESSION 16: THERMAL AND ELECTRICAL CHARACTERIZATION
Chair: Drew Hanser, *SRI International*

1:20 PM **16.1 Evaluating pHEMT Process Improvements Using Wafer Level RF Tests**
James Oerth, Stephen Cousineau, and Sushila Singh, Skyworks Solutions

1:40 PM **16.2 Degradation of pHEMT Performance in BiFETs Caused By Thermal History During HBT Growth on It, and Suggestion for Improvement**
Junichiro Takeda, Ryota Isono, Hiroyuki Kamogawa, Chihiro Hirooka, Masae Sahara, Jiro Wada, Shouichi Nagao, Yukio Sasaki, and Yohei Otoki, Hitachi Cable Ltd.

2:00 PM **16.3 Failure Investigations on AlGaN/GaN HEMTs for Different Sheet Resistances by Means of Raman Thermography**
Helmut Jung[1], Michael Hosch[2], Reza Behtash[1], James R. Thorpe[1], Franck Bourgeois[1], Stefanie Held[1], Herve Blanck[1], Andrei Sarua[3], Nicole Killat[3], Martin Kuball[3], and Thomas Roedle[4]
[1]United Monolithic Semiconductors, [2]Ulm University, [3]University of Bristol, and [4]NXP Semiconductors

2:20 PM **16.4 Accurate Non-Destructive Determination of the Lateral Thermal Conductivity of Novel Substrate Materials Using Thermal Indrared Microscopy**
E. R. Heller[1], K. Chabak[2], V. Miller[2], D. Walker, Jr[2]., M. Trejo[2], M. Kossler[2], J. K. Gillespie[2], A. Crespo[2], R. Vetury[3], and G. D. Via[2]
[1]Air Force Research Laboratory, Materials Directorate, [2]Air Force Research Laboratory, Sensors Directorate, [3]RF Micro Devices

2:40 PM **16.5 Continuous Improvement of Material Characterization Methodology Through Gage R & R Studies**
Arun Chawla, Mark Borek, and Guoliang Zhou, Skyworks Solutions

SESSION 17: DEVICE PACKAGING INNOVATION
Chair: Zaher Bardai, Epiphany

1:20 PM *Student Presentation*
17.1 Flip-Chip Assembled Ultra-Low Phase-Noise 7Ghz. InGaP HBT Oscillator
Li-Han Hsu[1,2], Dan Kuylenstierna[2], Herbert Zirath[2], Edward Yi Chang[1], and Chin-Te Wang[1]
[1]National Chiao Tung University, [2]Chalmers University of Technology

1:40 PM **17.2 EM Simulation adn Development of Wafer Level Micro-Packaging Technique for GaAs-Based RF MEMS Switches**
Sandeep Chaturvedi[1], Sangam V. Bhalke[1], Mahadeva Bhat K[2]., G. Sai Saravanan[1], R. Muralidharan[1], and Shiban K. Koul[3]
[1]Gallium Arsenide Enabling Technology Center (GAETEC), [2]Solid State Research Laboratory, Timarpur, and [3]Indian Institute of Technology - Delhi

2:00 PM **17.3 Novel Packaging Solutions for GaN Power Electronics: Silver-Diamond Composite Packages**
M. Faqir[1], T. Batten[1], T. Mrotzek[2], S. Knippscheer[2], L. Chalumeau[3], M. Massiot[3], M. Buchta[4], J. Thorpe[4], H. Blanck[4], S. Rochette[5], O. Vendier[5], and M. Kuball[1]
[1]University of Bristol, [2]Plansee SE, [3]Egide, [4]United Monolithic Semiconductors, and [5]Thales Alenia Space

2:20 PM *Student Presentation*
17.4 Quilt Packaging: A Coplanar Chip-to-Chip Interconnect Offering Ultra-Wide Bandwidth
David Kopp, M. Ashraf Khan, Scott Garvey, Kristen Anderson, Jason Kulick, Patrick J. Fay, Alfred M. Kriman, and Gary H. Bernstein, University of Notre Dame

2:40 PM **17.5 Cavity Structure GaAs FETs with High Humidity Resistance**
Yasuki Aihara, Toshiaki Kitano, Kazuyo Endo, Yoshiyuki Shehiro, and Kenji Hosogi, Mitsubishi Electric Corp.

SESSION 18: INTERACTIVE FORUM
Chairs: Suzanne Combe, *TriQuint Semiconductor,* and Andy Souzis, *II-VI Inc.*

3:00 PM - *Student Presentaion*
4:30 PM **18.1 Sub Half-Micron Structures with Profile Control on Compound Semiconductor Substrates Based on Conventional i-Line Lithography**
Dominik Schrade-Koehn[1], Philipp Leber[1], Herve Blanck[2], Hermann Schumacher[1]
[1]University of Ulm, and [2]United Monolithic Semiconductors

18.2 Backside SIMS Analysis and Accelerated Thermal Aging of Optimally Alloyed Ohmic Contacts to MESFETs
G. Sai Saravanan[1], Mahadeva Bhat K.[2], Sandeep Chaturvedi[1], M. N. Mudholkar[1], and R. Muralidharan[1]
[1]Gallium Arsenic Enabling Technology Center (GAETEC), [2]Solid State Physics Laboratory, Timarpur

18.3 Data Analysis for Yield Improvement Using TIBCO's Spotfire Data Analysis Software
Andrew Choo and Thorsten Saeger, TriQuint Semiconductor

18.4 LED Structure Grown on 200mm Sapphire Substrate
R. Schreiner, A. Boyd, O. Rockenfeller, J. Kaeppeler, B. Schineller, and M. Heuken, AIXTRON AG

18.5 TaN Resistor Process Development and Integration
M. J. Martinez[1], F. H. Austin[2], J. B. Clevenger[1], A. J. Grine[1], G. A. Patrizi[1], K. Romero[2], P. S. Vigil[2], S. Wolfley[1], and C. T. Sullivan[1]
[1]Sandia National Laboratories, and [2]LMATA

Student Presentation

18.6 N-Polar GaN-Based Highly Scaled Self-Aligned MIS-HEMTs with State-of-the-Art fT with LG Product of 16.8 GHz-um for Mixed Signal Applications
Nidhi, Sansaptak Dasgupta David F. Brown, Stacia Keller, James S. Speck, and Umesh Mishra, University of California, Santa Barbara

18.7 Peripheral Aspects for Utilizing the Full Benefits of SiC Power Devices
Peter Friedrichs, SiCED Electronics Development GmbH

18.8 Debris Reduction in GaAs Wafer Dicing Process
Kuan-Hsuan Ho, Shih-Ming Lin, Huang-Wen Wang, Kevin Huang, Ping-Wei Chen, and Chang-Hwang Hua, WIN Semiconductors

18.9 Numerical Analysis of the Effect of Grain Size and Defects on the Performance of CIGS Solar Cells
G. Sozzi, F. Troni, and R.Menozzi, University of Parma

18.10 Waste Reduction in Lapping Sapphire and Other Compound Semiconductor Materials
Elina Kasman and Mark Irvin, Engis Corp.

4.30 PM **CONFERENCE CLOSING RECEPTION**

SESSION 1: PLENARY SESSION

Chair: Marty Brophy, *Avago Technologies*

It's not easy being green.

- Kermit the Frog on "Sesame Street"

It is appropriate that our conference in Oregon, one of the greenest U.S. states physically and metaphorically, should begin with a pair of invited talks on how we can all be more environmentally sensitive in our fab operations. The conference starts off with a review of work led by Prof. David Johnson and colleagues at the University of Oregon and Oregon State University on how we can choose greener process options without loss of fab quality. Real process options creating much less waste promise to be both economically and ecologically advantageous. Passing then into the realm of large commercial fab operations, Steve Wooley, head of Workplace Services at Avago Technologies in Fort Collins, Colorado, discusses the broad-ranging and effective work on reducing waste, lowering water consumption, increasing recycling, and lowering energy usage in all areas of fab, test, and office operations. Many improvements in all parts of the whole operation are reviewed, many of which we could all easily do. This is clearly another example of how you can be environmentally proactive while maintaining and even improving your cost structure.

Moving into efficiency in design, the final paper of the opening session by a team from Delft University of Technology, UC San Diego, and Skyworks Solutions describes their path-breaking work on tuneable RF components. These enable high-speed adaptive filtering and matching permitting increased functionality, simplicity, and economy in RF systems. Semiconductor, MEMS, and Dielectric varactors and capacitive switch banks will be discussed and compared to new ultra-low distortion compound semiconductor varactors.

SESSION 2: RF MODULES

Chair: Yohei Otoki, *Hitachi Cable, Ltd.* and Earl Lum, *EJL Wireless*

Today we are living in the wireless world, which is filled with an ever expanding variety of cell phones, W-LANs, WWANs, GPS, and a host of other wireless appliances.

The application of these RF technologies continues spreading into new systems like smart grid and e-book and even into entertainment systems and toys. At the core of these wireless systems are RF modules which are powered and enabled primarily by Compound Semiconductor devices and packaged components and subassemblies of these. This special session will provide an up to date overview of the RF module manufacturing technology, as well as prospects for future directions for this industry. The session begins with an invited presentation by Mr. Ando from Navian who will provide a business overview and a description of the technical status and trends in the manufacture of RF modules. Next, we will have a panel session with panelists who are expert RF module engineers from Murata, AVAGO, TDK, Skyworks, RFMD and TriQuint. The panelists will give an overview of their products and describe some of the technical activities and challenges at their companies. They will describe what they expect and require from materials, at the device level, from the IC components, and from their packaging technologies. A lively and enlightening discussion is to be expected at in the question and answer period following the panel presentations.

SESSION 3a: BUSINESS ANALYSIS

Chair: Nick Kolarich, *Kopin Corp.*

The last year and half has been a roller coaster for our industry as the global economic recession set in and the future seemed uncertain. However, just as we cut back, out of nowhere the handset industry boomeranged back to record levels and is forecast by analysts to continue solid growth. To begin this session, Bruce Bernhardt from RIM (Research in Motion) will explain the rapid adoption of smartphones and other wireless devices which will continue to change the world in which we live. RIM is the leading manufacturer of smartphones for the US market, and his perspective gives us an inside track into RIM's outlook for the industry and what that means for compound semiconductors.

Along with rapid growth of wireless devices comes the necessary expansion of the infrastructure. Earl Lum of EJL Wireless Research will provide us with in-depth picture of the global base station market and the respective growth rates for 3G & 4G deployments. He will identify the leading OEMs and speak to the explosive demand for higher bandwidth and the evolving architectures being put in place. In addition, Earl will

cover the transition of this segment's business model from hardware to software, clarify the current state of the industry and how we might expect to see it evolve over the next few years, including free base stations!

SESSION 3b: TEAM TORTURE: DEVELOPING A STANDARD QUALIFICATION FOR POWER AMPLIFIER MODULES

Chair: Bill Roesch, *TriQuint Semiconductor*

This Panel will discuss the process of bringing together customer and supplier points of view in order to develop a JEDEC standard describing reliability requirements for the unique aspects of power amplifier modules. Each panelist will describe their suggestions for required tests, and their descriptions of weird and wacky stresses that are not so desirable. The panelists will elaborate on distinctive characteristics of power amplifier module qualifications, such as RF life testing, laminate-based packaging, and unique moisture acceleration factors, which justify the need for a special standard. Join this session to share your experience, offer advice, and learn from the panelists.

SESSION 4: DEVICE TECHNOLOGY

Chairs: Kamal Alavi, *Raytheon Corp.*

The Device Technology session has four regular papers and one interactive one, all having practical and relevant information for III-V device engineers. The first paper, from WIN, addresses the fabrication of high-yield 0.25um optical gate power pHEMTs at 8V drain bias, where low output power drift is achieved through epitaxial layer design optimization. The second paper, from IIT, India, and National Chiao Tung University, Taiwan, discusses a composite channel mHEMT with 78% Indium mole fraction for W band applications. The third paper, from GCS, details the performance status, and capabilities of double heterojunction InP/InGaAs foundry processing with fT and fmax higher than 250 GHz. The last paper, also from WIN, discusses the epitaxial design and device geometry for fabrication highly linear and thermally stable 0.5um optical gate FETs for wireless infrastructure applications. An additional paper on Device Technology is included in Thursday's poster session. The poster from Ulm University, in Germany, details the important topic of photoresist profile control for sub-0.5um T-gate formation using conventional i-line lithography tools.

SESSION 5: RELIABILITY

Chairs: Peter Ersland, *M/A-Com Technology Solutions*

This year's reliability session includes papers on both active and passive circuit elements, with relevance to both high volume consumer applications, and leading edge high voltage technologies. Our first paper describes an automated technique for characterizing the ruggedness of HBTs, an especially important parameter for GSM power amplifiers. The authors have used this technique to characterize different device designs, and will describe both the technique and their experimental results. Our second paper addresses the reliability of TaN thin film resistors as a function of temperature and current density. By performing reliability tests on resistors of various sizes the authors are able to better determine design rule limits for reliable resistor operation, leading to more compact circuit layouts. The third and fourth papers in this session address MIM capacitor reliability, particularly for use in high voltage MMIC technologies. The first of these discusses experiments performed to eliminate a low voltage failure population occurring at the edges of MIM capacitors. The authors identify both process and layout changes that lead to a reduction of these low voltage failures. The final paper of the session describes improved capacitor reliability resulting from the use of a new nitride deposition reactor. Comparing this new result to previous capacitor reliability tests, the authors show more than two orders of magnitude improvement in predicted capacitor lifetime, allowing long-term reliable operation at up to 50V.

In addition to this session, there are two reliability papers included in the poster session. The first of these describes a novel analysis technique used to determine the "as-processed" differences between stable and unstable ohmic contacts. The second presents the results of experiments performed to understand the root cause of early HBT failures during high temperature reliability tests.

SESSION 6: MANUFACTURING

Chairs**:** Jim Crites, *Cobham DES*

Sessions relating to manufacturing have always garnered a lot of interest in the community as these authors are sharing details on how they are in engaged in the day to day quest for manufacturing excellence.

The first paper in this session offers insight into planning and problem solving when an operating 4" manufacturing

site upgrades to larger wafer size. In this particular case it was a high volume HBT line and one of the key requirements was to make the transition seamless to the customers. From the complexity of tool conversion to the angst of throughput issues, this paper strives to offer a template for success.

Our next paper is a presentation on how a fab with older processing tools upgraded to allow for automation of process recipes and data monitoring. Tools without host computers were evaluated and creatively adapted to incorporate interlocks, barcode capability, or direct data transfer. In doing so, they have achieved a reduction of processing error rates and improved production yield.

Specialized material assessment is the topic of the next paper. Because channel sheet charge density is such a critical predictor for DC performance in pHEMT epi material, the authors of this paper devised a method to characterize the wafers without the need to sacrifice viable material. The ability to proactively adjust growth parameters has led to improved process output.

Next is a paper which aims at the heart of manufacturing excellence; determination of process shifts. While every tool or operation has some measurable outcome, many times it is determined only through the use of witness wafers or sacrifice of product wafers. Can one simple measurement gauge the variation of multiple parameters simultaneously? This paper advocates the utilization of carefully measured wafer mass to detect process shifts.

And finally, in a poster presentation at the Interactive Forum, is a paper devoted to extolling the benefits of on-line data analysis. Referencing a particular software package, the authors will elaborate on how easy access to manufacturing metrics can help improve productivity and yield.

SESSION 7: GaN GROWTH & CHARACTERIZATION

Chairs: Victoria Williams and Ruediger Schreiner,
AIXTRON AG

Since Nakamura's demonstration of the feasibility to establish a p/n-junction in wide band-gap GaN, new and different designs of material compositions and hetero-junctions for related compounds have demonstrated to open new pathways, whether being applicable for electronics or opto-electronics, and being possible for this direct material system due to, besides others, the controllability of band-gap engineering covering the range between 0.7 eV (InN) and 6.2 eV (AlN). This session will

provide an update on some of the subjects recent investigations have been focussing on.

The first presentation, by University of Fukui in conjunction with Japan R&D Center for Metal, Sharp Corporation, and Sumitomo Electric Industries explains that for HEMTs, the use of an AlGaN channel as part of the growth on free-standing AlN substrates, comparing it with standard AlGaN/GaN-HEMT on Si, is advantageous regarding high-temperature dependency of drain current degradation, on-state resistance, and threshold voltage, as well as reveals a one order of magnitude lower leakage current.

Initiatives to counter global warming strongly support lighting to switch from conventional devices over to GaN-based LEDs. AIXTRON will show that MOCVD growth of LED structures on 6 inch diameter sapphire substrates, as a strong request for cost reduction against growth on 2 inch, 3 inch, and 4 inch diameters before, can be achieved in an production environment, based on horizontal flow technology, speeding up process development, and time-to-market through simulation upfront, as well as using in-situ curvature measurement.

To establish and maintain device performance of HEMTs regarding thermal resistance, it is insufficient to only look on those parameters of the materials used. The University of Bristol will guide us to Benchmarking of Thermal Resistance of the GaN-SiC interface for AlGaN/GaN devices on SiC substrates. The importance of having a close look onto this will be demonstrated, comparing the results from investigations on materials from various suppliers, whether from the industry or R&D environment.

To take advantage of lower contact resistance and better electron confinement, as a requirement for ultra-high speed applications, University of California, Santa Barbara explored N-polar orientation GaN HEMTs allowing now re-growth of InP by MBE for the formation of an ohmic contact to metal, different than for standard Ga-polar. Further process fine-tuning, including the insertion of an InGaN graded layer between GaN and InN led to a HEMT device featuring a record low ohmic contact resistance value.

Poster Presentation:

Increase in diameter for epi-wafers as the starting material for the production of GaInN LEDs, has been the request from the beginning when only wafers of 2 inch in diameter were available, due to two major reasons: cost reduction for final device and compatibility with Si-technology. 200

mm diameter sapphire substrates were used for the growth of a generic LED structure in a vertical flow regime MOCVD system, taking advantage of in-situ tools for measurements of wafer curvature, as well as precise temperature profile across the wafer susceptor. Promising results for substrates made from sapphire will be presented, as well as those from Silicon, assuming that the latter results will be available by then.

SESSION 8: PROCESS METAL

Chair: Paul Werbaneth, *Tegal Corp.*

CS MANTECH, as a conference, is all about compound semiconductor *manufacturing* technology, and, in this year's metallization session, the emphasis is squarely on papers and topics from some of the world's powerhouse fabs reporting on the robust, cost-effective, solutions these fabs and engineers have developed to increase the productivity and yields of the metal processing steps employed in High Volume Manufacturing of III-V devices today. In the metallization session's first paper, Northrop Grumman Space Technology describe how wafer level bump technology developed on the silicon-side of the world can be successfully ported over into a III-V MIMIC backside metallization process. The benefits of wafer bumping include enabling both chip-level and wafer-level assembly of the MMIC devices, which reduces the overall assembly cost and enhances the RF performance of the "bumped" devices. In the second paper of this session, TriQuint Semiconductor report on their successful efforts to develop I-line negative photoresist lift-off processes for producing the very fine interdigital transducer metal structures that are the defining features of Surface Acoustic Wave devices. TriQuint's target: clean, wing-free liftoffs. Their results: SAW filter duty factors within 2% of target, and excellent liftoff process capabilities across a range of feature sizes. Converting TaN reactive sputter deposition processes from a batch tool to a single wafer tool is a project in itself. Converting TaN reactive sputter deposition processes from 4" wafers to 6" wafers? Another significant project. Doing both at the same time in a production environment? That's one for the professionals, and the subject of the third paper in this metallization session, presented by Skyworks Solutions (West Coast). The fourth paper in this session, from (East Coast) Skyworks Solutions, tells how Skyworks developed novel measures to prevent excessive cross-linking in lift-off photoresists as a result of secondary electron emission during lift-off metallization. The excessively cross-linked photoresist doesn't strip well, so residues seen post-strip can be directly correlated to the amount of secondary

electron generation during E-beam metal evaporation – a valuable observation, and one necessary for reducing the amount of said post-strip residues, thereby increasing device yields and reducing fab cycle times. The Metallization Session finishes with a talk from Avago Technologies and WIN Semiconductor on improved emitter resistance achieved through using barrier metals in an InGaP HBT process. Using STEM and flyback measurement techniques, Avago and Win show how sputtered barrier layers of either TiW or W affect the stability of InGaAs – barrier metal – Ti interfaces, and how the barrier layers reduce mean flyback resistance, and also greatly improve the overall distribution of the flyback resistance results.

SESSION 9: GaN DEVICE MANUFACTURING

Chairs: Scott Sheppard, *Cree, Inc.*

The GaN Device Manufacturing session contains four regular papers and one student paper that each address different aspects of GaN HMET device manufacturing: process intolerance to variable free-standing wafer shape, improved ohmic contacts, threshold voltage control, improved metal liftoff and MMIC technology. The session begins with a discussion from P. Kurpas of FBH-Berlin on a method to process and benchmark GaN devices on wafers from various epitaxial vendors who deliver a broad range of bow and/or irregular shapes. The second paper from H. P. Xin of Northrop Grumman Space Technology covers an exciting overview of AlGaN/GaN HMET ohmic contacts that are optimized for improved surface morphology with low contact resistance, which is a crucial topic for proving that GaN is truly manufacturable. Third in line is a student paper from H. Chen at Hong Kong University of Science and Technology. This is a very clever report showing the manufacturability of enhancement mode GaN HEMT devices can be achieved using the extremely mature technology of threshold voltage control by selective ion implantation. Next will be a regular paper from R. Behtash of United Monolithic Semiconductors, explaining their method to remove metal skirts from thick evaporated Au stacks. This manufacturing solution to a tough problem offers promise for improved device performance. Completing the session will be an overview from P. Waltereit of Fraunhofer-Freiburg of X-band MMIC processing and performance. He reports on device performance and reliability of their 3-inch GaN HEMT and MMIC technology on SiC substrates.

SESSION 10: PROCESS ETCH

Chairs: Russ Westerman, *Plasma-Therm LLC,* and Chris Yousey, *Microlink Devices*

Papers in this section focus on practical problems that arise during wet and dry etching of compound semiconductors and the solutions used to overcome them. The first paper of the session by Skyworks Solutions discusses a yield loss problem related to a dry etch process for polyimide vias. The cause of the yield loss was found to be a reduction in process margin due to an interaction between a resist material change in conjunction with substrate heating during a dry etch process. The second paper in the session by the U.S Army Night Vision & Electronic Sensors Directorate investigates the use of optical emission spectroscopy (OES) during the dry etch of HgCdTe devices. Relative emission intensities for various reactants and etch products are correlated to etch performance in an effort to understand the interaction of resist profiles, materials and plasma parameters during HgCdTe device processing. The next paper by Plasma-Therm also looks at using plasma emission to control compound semiconductor dry etch processes. The theory, application, and limitations of optical emission interferometry (OEI) are described along with data demonstrating the capability of OEI to endpoint etch processes at specific material interfaces after a given etch depth into a material has been achieved. The final two papers of the session focus on wet etch processes. Cobham looks at yield losses during microwave FET processing due to electrochemical etching near the transistor gate. Information related to the process sequence as well as the corrective actions to the process are disclosed. In the final presentation, a team from Sandia National Labs looks at surface treatments to improve wet etch performance during base-collector formation for HBT fabrication. A NH_4OH based pretreatment to remove native oxides prior to lithography was found to improve resist adhesion, sidewall profile, and ultimately the step coverage of subsequent interconnect metallization.

SESSION 11: EMERGING GaN-BASED BARRIER STRUCTURES

Chair: Dave Via, *Air Force Research Laboratory*

AlGaN/GaN HEMT technology has matured significantly over the past few years with many companies now offering a variety of discrete devices and circuits for power amplifier applications. While this technology offers significant advantages in power density and total power over competing technologies, performance is generally

limited to Ka-band and below. New GaN-based barrier structures are being explored that will enable higher power levels at higher frequencies and offer new application opportunities such as enhancement mode operation.
The first paper of the session comes from the Sensors Directorate of the Air Force Research Laboratory at Wright Patterson AFB, OH. James Gillespie will describe recent work on InAlN barrier structures. Growth, materials characterization, device fabrication, and test results will be discussed. The second paper is a student paper and comes from Dr. Tomas Palacios' group at the Massachusetts Institute of Technology. Han Wang will discuss the work at MIT exploring the design space of InAlN/GaN devices through a study of the scaling behavior of $In_{0.17}Al_{0.83}N$/GaN HEMTs as a function of InAlN thickness, gate recess and gate length. Record transconductance results will be presented. The third paper of the session, also a student paper, comes from Dr. Umesh Mishra's group at the University of California, Santa Barbara. Man Hoi Wong will describe the N-polar growth being investigated at UCSB. These GaN/AlGaN HEMTs may provide a solution the problems of poor electron confinement and high ohmic contact resistance in highly-scaled GaN transistors since the two-dimensional electron gas (2DEG) is induced on top of the heterojunction. Power and efficiency data will be presented. The fourth paper, the final student paper of the session, comes from Dr. Huili Xing's group at the University of Notre Dame. Chuanxin Lian will discuss how the group at Notre Dame is using selective area regrowth to overcome the difficulty in achieving ohmic contacts in AlN/GaN HEMTs. Process flow and contact optimization results will be presented. The final paper of the session is from the Naval Research Laboratory in collaboration with the University of Maryland. Travis Anderson of NRL will describe a novel AlN/ ultrathin AlGaN/GaN HEMT structure that is being explored which will enable enhancement mode operation. The fabrication process and device results will be discussed

SESSION 12: EMERGING TECHNOLOGY A

Chair: Amy Liu, *IQE, Inc.*

Three presentations in session 12 describe novel device concepts while the invited paper from Osaka University covers the exciting luminescent and magnetic properties of rare-earth doped semiconductors and their application to GaAs-based 1.5µm and GaN-based red LEDs. The invited paper from Penn State University will address important aspects of CS-based tunnel transistor architecture for energy efficient logic applications, addressing both

theoretical considerations such as switching speed as well as fabrication and characterization of such devices. The presentation from GA Tech will demonstrate advancements on III-N DHBTs through the use of higher In content in the base layer, and discuss both fabrication technique and device analysis. Finally, the work from the University of Notre Dame will show the promise of enhancement-mode InAlP-oxide gate pseudomorphic MOSFETs. These are attractive device candidates for future high-speed circuits enabling the design of circuits operating from a single power supply.

SESSION 13: GaN POWER SWITCHING

Chair*:* George Henry, *Northrop Grumman ES*

With each passing year the promise perceived for wide band gap semiconductor devices becomes more a reality as prototype devices are steadily transitioned to products. This session focuses on high power switching capabilities. In our opening invited paper, Michael Briere of ACOO LLC Enterprises presents an exciting vision of a future where adoption of efficient wide band gap devices for power electronics is widespread. According to Dr. Briere, this can result in a 25% reduction in worldwide power consumption in 2025 and an attendant reduction in the need for new power plants. Following this, Marianne Germain of IMEC discusses progress in her lab in the development of III-N devices for price-effective power devices using GaN-on-Si up to 200mm diameter. Significant progress has been achieved using DHFET (SiN/AlGaN/GaN/AlGaN) with *in situ* SiN acting as an additional part of the barrier, defining the 2DEG. Dr. Germain will discuss this and progress towards Si-CMOS-compatible GaN-on-Si. Moving from these broad perspectives to the practical issues of power device fabrication, our next paper, presented by Ogyun Seok of Seoul National University, shows that by using rf-pecvd-deposited diamond-like carbon for passivation an impressive breakdown > 1400V can be achieved for AlGaN/GaN Schottky Barrier Diodes. Next Chunhua Zhou of HKUST reports that by combining enhancement and depletion mode channels on a Lateral Field Effect Rectifier, a 53% lower on-resistance can be obtained (compared to a conventional L-FER) while maintaining equivalent punch-through immunity. Finally, Minki Kim, also of Seoul National University, describes an AlGaN/GaN power HEMT with a gate edge recess. Compared to a FET without this recess, the breakdown voltage is raised by 100V and the leakage current reduced by an order of magnitude with only a slight reduction in current.

SESSION 14: EMERGING TECHNOLOGY B

Chair: Andreas Eisenbach, *IQE plc*

The invited presentation from UC Berkeley will discuss recent advances in SiC-based MEMS for harsh environment sensors where the use of Si is no longer feasible; covering various manufacturing aspects from growth through micro-machining to contact properties. In recent years, photovoltaic technologies have shown exciting progress in the push for the use of renewable energy. Oerlikon Solar's paper will outline the three major Thin Film Technologies and respective financial and technological roadmaps in the near future. The final two presentations of this session will cover novel aspects of LEDs; UIUCs paper will show advances in LEDs for short-range data communication through increased modulation speed, while the paper from NTU will demonstrate their improved fabrication methods for GaN nanorod LEDs resulting in higher output power, lower leakage, and more uniform light emission.

SESSION 15: BACKSIDE PROCESSING

Chair: Michelle Bourke

For years there have been backside processing sessions at ManTech. In earlier years it was GaAs then we had a brief flutter of papers relating to InP and last year we had several papers on SiC. This year's backside session has a balance between GaAs and SiC.

The session begins with an exciting paper from Fujitsu Limited and Fujitsu Laboratories Ltd. The paper discusses the process issues relating to the wafer support for SiC via etching and wafer dicing for GaN HEMT MMICs with 0.1µm length gates and a very thin SiN passivation layer. The second paper is a joint paper from United Monolithic Semiconductors and Fraunhofer Institute for Reliability and Microintegration. A Mobile Electrostatic Carrier (MEC) for the temporary bonding of thin GaAs wafers using an electrostatic force for processing and handling in a manufacturing area will be presented. The next paper comes from TriQuint Semiconductor in Texas and reviews the effects of the various process parameters on pillar formation in SiC vias. Optimised process conditions will demonstrate a SiC backside via manufactured at relatively low temperatures. The final paper in this session comes from Mitsubishi Electric Corporation and investigates the use of Ni-P as a seed layer prior to Au plating. The Ni-P

causes stresses in the wafer. This paper will show the causes of this stress and a process that has been introduced to reduce it.

SESSION 16: THERMAL AND ELECTRICAL CHARACTERIZATION

Chair: Drew Hanser, *SRI International*

Presentations in this session focus on understanding the thermal and electrical behavior of devices and their impact on process control and device performance. A multinational collection of researchers will share their findings in these important areas. The first paper in this session, from Skyworks Solutions, Inc., addresses wafer level RF testing to provide more rapid process feedback and to increase production capacity and capabilities. Hitachi Cable Ltd. will then share results investigating the degradation in pHEMT performance in BiFETs due to their thermal history, clarifying the cause of degradation and proposing improvements. Following that, a research group headed by United Monolithic Semiconductors GmbH will present results from failure investigations in AlGaN/GaN HEMTs where they correlate the device temperature limit as measured by Raman thermography with the 2DEG sheet resistance of the device. In the next paper, researchers from the U.S. Air Force Research Laboratory and RF Micro Devices also investigate thermal effects in GaN materials and share IR measurements of heat spreading in GaN, presenting comparisons using different substrate materials. Finally, Skyworks presents a study investigating the repeatability and reproducibility of several measurement techniques for large-scale epitaxial wafer manufacturing, and introduces approaches to identify and address sources of measurement variation.

SESSION 17: DEVICE PACKAGING INNOVATION

Chair: Zaher Bardai, *Epiphany*

This session will focus on packaging developments for III-V devices, extending from RFMEMS switches and low phase noise oscillators to high speed communication integrated circuits and high power GaN devices. The discussions will include wafer level packaging using adhesive bonding techniques, semiconductor and Pyrex glass caps, flip-chip assemblies, polymer cavity structures that provide high humidity resistance in operating environments and, the use of silver diamond base materials for high power applications.

Special Thanks to our 2009 Exhibitors

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GENERAL INFORMATION

2010 International Conference on Compound
Semiconductor Manufacturing Technology
May 17th – May 20th, 2010
Portland Marriott Downtown Waterfront
1401 SW Naito Parkway
Portland, Oregon 97201

REGISTRATION INFORMATION (US$)

	On or before Apr. 20	After Apr 20
Full Conference Registration	$525.00	$625.00
Student Conference Registration	$125.00	$125.00
Government Conference Registration	$525.00	$525.00
One-Day Conference Registration	$300.00	$300.00
**** New Low Price ****		
Workshop Registration	**$175.00**	**$275.00**
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Payment of the full, student, or government conference registration fee includes one copy of the printed Conference Digest (if desired), one copy of the Conference Digest on CD, and admission to all sessions and the exhibits. It also includes the International Reception, Exhibits Reception, Exhibits Luncheon, Panel & Rump Session Reception, Interactive Forum Reception, continental breakfasts, and refreshment breaks. Additional copies of the Conference Digest may be purchased at $140.00 each. Additional copies of the Conference Digest on CD may be purchased for $50.00 each.

The one-day registration includes admission to all sessions for that day, admission to the Exhibits Hall, buffet breakfast, break refreshments, and lunch. The Rump Session Reception or Interactive Forum Reception is included on Wednesday and Thursday, respectively. It also includes a printed Conference Digest and a Conference Digest on CD. The one-day registration does *not* include admission to the International Reception. The one-day option can be taken only once during the conference.

Payment of workshop registration includes one copy of the Workshop Digest, continental breakfast, Workshop Luncheon and break refreshments. Additional copies of the Workshop Notes may be purchased at $100.00.

Registrants may pay by check, money order, bank draft or credit card. Make checks payable in U.S. dollars drawn on a U.S bank to: "GaAs MANTECH, Inc." Your name and address must appear on checks, money order or bank

drafts. The only acceptable credit cards are Master Card, VISA, and American Express. REGISTRATION FORMS SENT WITHOUT PAYMENT WILL NOT BE ACCEPTED. All refund requests must be received by Celicia Dell-Morrow at the CS Mantech office shown below by April 20th for a full refund less a $25 processing fee. **NO REFUNDS AFTER APRIL 20th.**

CS MANTECH
14525 SW Millikan Way #26585
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For Advanced Conference Registration, register online at our Web Site by April 20th.

www.csmantech.org

HOTEL RESERVATIONS

A block of rooms at the Portland Marriott Downtown Waterfront has been reserved for CS MANTECH participants and their guests. The special CS MANTECH room rate is $149.00 for single or double occupancy. Occupancy taxes (currently 12.5%) will be added to these rates.

To make a hotel reservation, please register online through our website at:

www.csmantech.org

Or Reservations can be made by calling toll free: 1-800-228-9290 within North America. Please be sure to mention you are a CS MANTECH attendee.

We ask you to please support CS MANTECH and to enjoy all of the conference activities by staying at our official 2010 location, the Portland Marriott Downtown Waterfront.

Hotel reservations must be received BEFORE Tuesday, April 20, 2010 to qualify for a room in the CS MANTECH room block. The discounted rate is subject to availability, so please MAKE YOUR RESERVATION EARLY! An advance deposit or credit card is required to hold your room.

Reservations received after Tuesday, April 20, 2010 will be accepted on a space- and rate-availability basis.
If the room block fills prior to the cut off date, reservations will be accepted based on space and rate availability, so RESERVE EARLY!

CONFERENCE REGISTRATION & INFO CENTER

Conference registration will open in the Ballroom Foyer on Lower Level 1 of the Portland Marriott Downtown Waterfront on Sunday night and will be open Monday through Thursday during the following hours:

Sunday	May 16th	5:00PM – 8:00PM
Monday	May 17th	7:00AM – 7:00PM
Tuesday	May 18th	7:00AM – 11:00AM 1:00PM – 5:00PM
Wednesday	May 19th	7:00AM – 5:00PM
Thursday	May 20th	7:00AM – 9:30PM

A Conference Attendee list will be available at the Information Center on Thursday, May 20th.

MESSAGE BOARD

A Conference Message Board will be maintained at the Registration & Information Center during registration hours. Please advise callers who wish to reach you during the day to ask the hotel operator to deliver a message to the CS MANTECH Conference Registration Desk. Please check the message board periodically.

SPEAKER PREPARATION ROOM

The Salmon Room on the Third Floor has been reserved for speaker preparation. This room will be open from 7:00 AM to 5:00 PM on Monday through Thursday, May 17th - 20th. The room will be set up with appropriate previewing equipment.

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Portland Marriott Downtown Waterfront
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General Information: 503-226-7600
General Fax: 503-226-1209

The 2010 CS MANTECH Conference will be held at the Portland Marriott Downtown Waterfront Hotel in Portland, Oregon. The City of Roses, one of the US's most livable cities, is a melting pot of ideas and wonder. From majestic mountains to sparkling waters, sumptuous restaurants to unlimited culture, lively entertainment to high-tech industry, Portland is unforgettable.

The Portland Marriott Downtown Waterfront Hotel is best known for our award-winning service, and now, guests of our downtown Portland, Oregon, hotel will love us even more after a recent $8.5 million renovation. Our downtown Portland hotel rooms now include 32-inch LCD TVs, modern bathroom decor, local artwork, and wireless internet. Guests at our hotel will enjoy our indoor pool, whirlpool, on-site fitness center, and nearby golf and spas. Business travelers will appreciate our downtown Portland hotel's 24,000 sq ft of meeting space, spacious work desks, and 24-hour business center. Dining options are provided in Allie's American Grille and Champion's Sports Bar where you can watch and cheer on the Oregon Ducks as they play Ohio State in the Rose Bowl on any number of TVs. One of the few hotels in downtown Portland, Oregon, earning the prestigious ENERGY STAR label and is Green Seal Silver Certified for its efforts to protect the environment. Plan your next stay at our eco-friendly downtown Portland hotel!

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or click on the hotel link at
www.csmantech.org.
For more information on Portland activities, visit
http://www.travelportland.com/visitors/

TRANSPORTATION TO THE HOTEL

Portland Airport- PDX
Hotel direction: 9 miles SW

Driving Directions: Take Airport Way East to I-205 South. Then take I-84 West to the City Center (City Center/Oregon City)exit, continue to follow signs to City Center. Cross Morrison Bridge and take Naito Parkway Exit and turn right. Hotel is 1/2 mile on right. //Northbound on I-5: Take City Center/Naito Parkway Exit. Go through 2 stoplights; hotel is directly on right.

This hotel does not provide shuttle service.

Alternate transportation: Blue Star (503) 249-1837;
Fee: $14.00 (one way) reservation required

Light-rail service, fee: $2.55 (one way)
www.tri-met.org

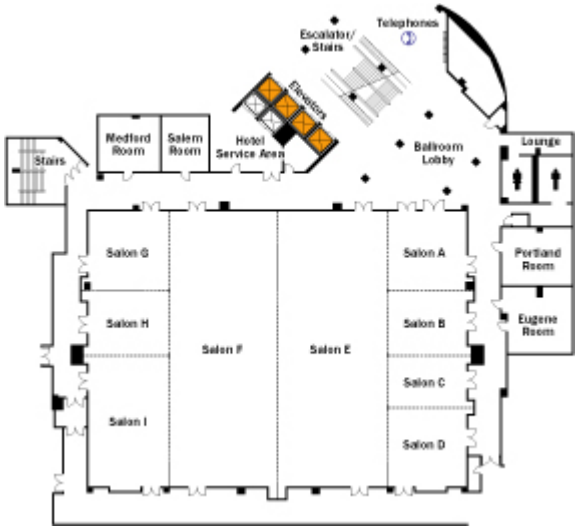
Estimated taxi fare: $35.00 (one way)

FINANCIAL ASSISTANCE

CS MANTECH strongly encourages and supports participation from academic delegates. Students and University Professors seeking financial assistance should contact Mariam Sadaka, the 2010 University Liaison, by email at student.aid@csmantech.org.

Portland Marriott Downtown Waterfront

MEETING ROOM LAYOUT



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