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TCAD Simulation of Compound Semiconductor Electronic Devices

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Objective of Workshop

This workshop will begin with a review of the fundamentals of TCAD simulation and available tools. DC and small signal AC simulation of devices will be discussed in detail. There will be a focus on calibration and the meaning of that calibration. The fundamentals of heterostructure simulation will be presented with examples.
Outline of Workshop

► Vendor review
► Objective of simulation
► General simulation flow
  • Process simulation
  • Gridding
  • Device simulation
    ▪ Heterostructure simulation
    ▪ Convergence
    ▪ Transport options
    ▪ Trap models
    ▪ Stress
    ▪ Quantum correction
    ▪ Material properties
    ▪ Special topics
      – Gate leakage
    ▪ Solutions in TCAD
    ▪ DC Simulation syntax
    ▪ Mixed mode

► Examples
  • Objectives of simulation
  • HBT
  • GaAs MOSFET
  • Switch transient simulation under mixed mode
  • Large signal
Objective of TCAD simulation

► What can TCAD do
  • Provide a technical best prediction of DC, AC and transient performance

► Worst kind of TCAD problem
  • “I saw something funny in the data, run some simulations and tell me what’s causing it”

► In TCAD simulation is a prediction based on physics and geometry
  • Predictions are limited to data supplied and physical mechanisms included
  • When some of the key mechanisms are not well understood …
  • There are often clever ways to make predictions when some of the mechanisms are unavailable or when key parameters are unknown, but not always

► When TCAD is used to solve a problem the most critical step is to demonstrate the problem in TCAD
  • If you can’t simulate the problem, it may be difficult to use TCAD to find the problem or simulate the solution
Objective of TCAD simulation

The objective of TCAD is to leverage prediction to solve problems that lead to better technologies

- Since prediction is the objective then it is important to understand the concept of prediction

  ▪ Compact models are fit to a training data set, they can then predict the performance of a device ~within the range of the training data set

  ▪ TCAD is calibrated to a dataset,
    - Predictions are then based on a physical description of the gridded device and physical mechanisms applied at those grid points
    - We can presume that the TCAD solution can be used to do prediction outside the range of the calibration data set, but
    - The farther we get away from that calibration data the more risky the prediction
    - This is because there are approximations in the formulation and the calibration eliminates the offset associated with these approximations locally
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TCAD Tools

► Major tool TCAD tool vendors
  • Synopsys bought ISE (Integrated Systems Engineering) in 2005
  • The tool set is essentially the original ISE toolset with the new name Sentaurus
    ▪ A typical simulation would have these elements
      – S-Process (Floops) -> S-Edit (Devise) -> S-Device (Dessis)
  • Silvaco
    ▪ Similarly
      – Athena -> Devedit -> Atlas
  • There are numerous University codes, these may be useful but don’t typically have the features that make simulations possible in real problems
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What do these tools do?

- Process
  - As closely as is reasonable fabricate the device in simulation
    - In Silicon simulation process is the challenge, in compound semiconductors the greater challenge is typically in the device simulation
  - Retain as many details as possible
    - That makes it possible for you to use simulation to create spots on those process steps
  - The tools are designed mostly for silicon simulation so there are compromises

Example from Silvaco’s Athena
Process simulation

There are two potential objectives of process simulation

1. Investigate the process, and its variability using process simulation for development, (this is common in development of Silicon devices, not so much in development of compound semiconductor devices)

2. Build a structure that accurately describes a device for device simulation, this is more common in compound semiconductors, this can be done in three ways
   1. A full process simulator (Athena or S-Process)
   2. By importing some measured profiles into a structure
   3. By using an edit program to draw the device and then drop in measured or conceptually determined profiles (Devedit, or S-Edit)

Example from Silvaco’s Athena
Process simulation

► Process simulation emulates actual fabrication
► There are commands to deposit layers, define doping, create implantation profiles, mask off, and etch layers
► Each of these steps has a thermal budget where defined diffusion mechanisms are used
► Movement of dopant species is described by these diffusion steps

► In Heterostructure simulations elements diffuse across material boundaries creating new mixes of materials but this isn’t taken into account in commercial simulators
  • For example at AlGaAs InGaAs boundary there is diffusion of Al, In, Ga, As, these diffusions are typically small and the impact of a thin InAlGaAs interface material between the AlGaAs InGaAs is not considered

► Crystallographic etching isn’t typically taken into account either
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Creating a grid

► Edit

- The process grid is not well designed for device simulation so the device must be re-gridded after process simulation specifically for device simulation
- Gridding is very important, and
  - there doesn’t seem to be analytical solution for compound semiconductors
  - most grids require manual intervention
- What is important in gridding?
  - Need enough grid points to
    - Make the solution grid independent
    - To accurately describe your device
      - Remember the device is only described in the simulator at the grid points
  - More grid points are not always good
    - The grid becomes stiffer
    - The simulation gets a lot slower
  - You want the smallest number of grid points that is sufficient to describe the solution
  - Your grid will be mechanism dependent
  - If there are surface traps - decrease the vertical grid spacing at the surface to describe the trap depletion
Gridding problems

► There isn’t a fool proof analytical gridding algorithm for compound semiconductor devices that I am aware of

  • Manual grids are common
  • You need a gridding philosophy for your device
  • The grid spacing should be smaller at vertical and horizontal discontinuities
  • Once a grid exists you may have problems getting convergence
    ▪ Run some tests with gridding options, this can be parameterized so that it can be done in parallel on a compute farm
    ▪ You may be able to run a simulation up to the point where convergence fails and then save the output
      – Plots of the internal characteristics of the device at this point may reveal the issues
      – There are ways to dump out the location of the largest update which helps in finding the problem, and which equation is not converging
      – Changes to the math, solver, or implementation of the physics may be tried
        ► Solver, and math issues
        ► Highly doped semiconductors
        ► Grid adaptation is incompatible with heterostructures (AGM) (chapter 30)

  • Just remember, mistakes often show up as convergence problems
Gridding case study

Device: GaAs Gadolinium Gate Oxide FET
Models, hydrodynamic, and density gradients
Convergence is difficult in drain sweeps when there is very low current

- Solutions
  - Sweep the gate to turn on the channel before sweeping the drain
  - Decrease lateral grid spacing – slower solution

- Next step after getting good convergence
  - Build a parallel study in which you increase the grid spacing in high grid count regions
  - A courser grid isn’t as stiff, and generally converges better overall
  - Solution cutbacks occur when convergence fails
    - These cutbacks take more time than a large grid would take
    - Very small minimum cutbacks (where convergence would fail) are seldom the solution
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How do you describe a device in some materials system in a device simulator?

- You describe the conduction (valence) band in terms of the electron affinity of each material.
- This allows the simulator to construct a model of conduction band discontinuities.

- Poisson is then used to determine the potential due to charge.
These two solutions are added together to give the vertical potential profile

As we will see this is described only at grid points

When there are quantum effects quantization impacts the charge profile and the resulting electric potential solution
Device Simulation

Device
- Ah, there’s the rub!
- Device simulations
  - Material parameters
  - Mechanisms
    - Transport
    - Quantum
    - Recombination
    - Traps
  - Coupled equations are solved using a Newton’s method approach
    - The more effects included, the more equations, the more memory and the more time required
  - Transport mechanisms, Poisson, Quantum – solve multiple eqns
- DC
- AC
- Temperature
- Mixed mode

Drift diffusion, or Hydrodynamic drive

Schroedinger solver, or Density Gradients

Fixed or Hydrogenic
Solve {
  Poisson
  Coupled {Poisson Electron}
  Quasistationary (Goal { Name="gate" Voltage=2 })
  { Coupled {Poisson Electron} }
}

Hydrodynamic – solution based on Boltzmann transport considering energy of carriers
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Convergence control

► RefErrControl
► RhsFactor maximum change to allow the same Jacobian to be used
► ErrRef(electron)=1e7
► ErrRef(hole)=1e7

► Keep good records, change one thing at a time, maintain the ability to back up one step when you make it worse
  • Impatience is your enemy

\[
\left| \frac{\Delta x}{x} \right| < 1
\]

\[
\varepsilon_R \left| \frac{\Delta x}{x} \right| + \varepsilon_A < 1
\]

\[
\varepsilon_R = 10 - \text{Digits}
\]

\[
\left| \frac{\Delta x}{x} \right| < \varepsilon_R
\]

\[
\left| \text{Rhs}_k \right| < \text{RhsFactor} \cdot \left| \text{Rhs}_{k-1} \right| \quad (17)
\]

\[
\left| \text{Update}_k \right| < \text{UpdateFactor} \cdot \left| \text{Update}_{k-1} \right| \quad (18)
\]
Transport Options

► “I just want to get a quick answer, use drift diffusion”
  • What difference does it take how long it takes to get the wrong answer?

► There are many opinions on drift versus hydrodynamic drive and much of that comes from Silicon experience
  • In some software there are issues with the high field saturation model in barrier materials when using drift diffusion in heterojunction devices

  • Hydrodynamic drive provides a solution to Boltzmann transport equation (BTE) using the relaxation time assumption
  • Drift diffusion solves for the field at each point in a device and then determines current, impact ionization … from those fields, problem is they are really determined based on electron energy not the local field
  • Hydrodynamic drive/Energy balance approaches solve for electron energy
Velocity models

► Mobility models
  • You can specify a mobility, a mole fraction dependent mobility
  • You can also specify a doping dependent mobility

► Velocity models
  • There are two choices for velocity models for compound semiconductors
    1. A saturation model that looks a whole lot like silicon
      1. This is $v_{sat} = 2$
    2. Energy dependent mobility model,
      1. more complex, and harder to use

► Relaxation times
  • There are two choices
    1. A constant relaxation time
      1. This and a constant saturation velocity may lead to an unrealistic transport picture
    2. Energy dependent relaxation times
      1. more complex, and harder to use
The high field velocity model for GaAs is shown in the blue curve.

This model has negative differential mobility (NDM).

A saturated velocity model, similar to that seen in Silicon is shown in red.

Typically this saturated velocity model is used instead of the NDM model because of complexity.
Negative differential mobility - energy dependent relaxation time model

- Must include energy dependent relaxation times
Energy relaxation rate

- Assuming constant relaxation time
- GaAs Energy dependent relaxation time (EDRT)

\[
\frac{dW_n}{dt} = \left( \frac{3}{2} k \frac{T_n - T_L}{\tau_{en}} n + \frac{3}{2} k T_n R_{SRH} \right) \lambda_n + E_x \left( G_n - R_n^4 \right)
\]

\[
R = \frac{W_n - W_0}{\tau}
\]
Energy vs Field

GaAs, AlGaAs, and InGaAs
Trap models

► Trap types
- Traps are a big deal in compound semiconductors
  - They can be defined in a bulk or at an interface

- Fixed, Acceptor, Donor, neutral traps
  - Fixed traps are constant amounts of charge, typically at an interface
    - They reflect a circumstance in which the trap is always completely occupied
    - Note that these are static traps that change are dynamic, or transient because they change over time based on changing bias conditions
  - Acceptor and eNeutral traps
    - Uncharged when unoccupied and carry a charge of one electron when occupied
  - Donor and hNeutral traps
    - Are uncharged when unoccupied and they carry the charge of one hole when fully occupied

► Traps can be defined with different distributions of charge, the most common is Gaussian, but table input is also interesting

\[ n = N_0 e^{-\frac{(E - E_0)^2}{2E_s^2}} \]

► \( N_0 \) is the concentration, \( E_0 \) is the center of the trap energy distribution, and \( E_s \) is the sigma
Density Gradient Model

- Density Gradient
- Where \( n \) is the charge density
- \( m_n \) is the effective mass

\[
\beta = \frac{1}{kT_n} \\
\Phi = E_C + \Phi_m + \Lambda_n \\
\Phi_m = -kT_n \ln \left( \frac{N_C}{N_{\text{ref}}} \right) \\
\Lambda_n = -\frac{\gamma \hbar^2}{12m_n} \left\{ \nabla^2 \ln n + \frac{1}{2} \left( \nabla \ln n \right)^2 \right\} = -\frac{\gamma \hbar^2}{6m_n} \frac{\nabla^2 \sqrt{n}}{\sqrt{n}}
\]
In many structures quantized wells are used. This is particularly true of HEMT structures where charge is placed adjacent to the channel and the mobility of the channel is maintained. Due to quantization the charge in the channel does not look like it would under a semiclassical setting (shown in blue). Schroedinger Poisson can be used to solve for this charge (shown in red). The density gradient model can be used to give this same model.
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• Typical electric field profile

structure at off-state breakdown structure at on-state breakdown
This slide shows the calibration between simulated and measured 2 terminal breakdown current as a function of temperature from 25 to 150°C. The mechanisms are impact ionization and thermionic field emission.
This is an illustration of the proposed gate to drain breakdown mechanism. Here electrons tunnel in along the gate due to high reverse fields. Tunneling is anticipated to occur for fields near 1e6 V/cm [Robbins, 1988 #3].

Impact ionization occurs in AlGaAs and InGaAs material below resulting in holes that escape to the gate, populate surface states altering channel depletion and degrading performance, and escape to the substrate.

Neither mechanism alone accounts for the current observed in measured data because the tunneling mechanism feeds carriers to the avalanche mechanism
Impact Ionization Parameters

► Impact ionization generation
► GaAs

► AlGaAs in 10% molefraction increments
► InGaAs 20% molefraction
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How does it work?

► Solver runs a coupled solve of several equations describing the problem
► Each additional equation adds to the size of the problem and the solution time.
► For a problem there are the number of grid points times the number of equations to be solved

\[
\text{Poisson: } \nabla \cdot \varepsilon \nabla \phi = -q \left(p - n + N_D - N_A\right) - \rho_{\text{trap}}
\]

\[
\text{Continuity: } \nabla \cdot J_n = q R_{\text{net}} + q \frac{dn}{dt}
\]

\[
\text{Drift Diffusion: } J_n = -n q \mu_n \Phi_n
\]

\[
\text{Hydrodynamic: } J_n = q \mu_n \left(n \nabla E_c + k T_n \nabla n + f_{n}^{\text{id}} n k n \nabla T + \frac{3}{2} n k T_n \nabla \ln m_n \right)
\]

\[
\text{Density Gradients: } \Lambda_n = \frac{\gamma h^2 \nabla^2 \sqrt{n}}{6 m_n \sqrt{n}}
\]

► LU decomposition of the Jacobian is typically done

\[
J_F(x_n)(x_{n+1} - x_n) = -F(x_n)
\]

\[
x_{n+1} = x_n - J_F(x_n)^{-1}F(x_n)
\]
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Electrode {
   { Name="Source" Voltage=0 Resistor=417}
   { Name="Drain" Voltage=0 Resistor=417}
   { Name="Gate" Voltage=0 WorkFunction=5.2 Resistor=300 }
   { Name="substrate" Voltage=0 schottky barrier=0.7 }
}

File {
   Grid = "input/ggofet_mdr"
   Doping = "input/ggofet_mdr"
   Current = "d_ox/plot"
   Output = "d_ox/log"
   Plot = "d_ThuFeb15122658200719/dat"
   Parameter = "../../common_files/specific.par"
}

Plot {
   EtappedCharge
   Egapstatesrecombination
   htrappedcharge
   hgapstatesrecombination
   Potential Electricfield
   eDensity hDensity
   eCurrent/Vector hCurrent/Vector
   TotalCurrent/Vector
   SRH Auger
   eMobility hMobility
   eQuasiFermi hQuasiFermi
   eGradQuasiFermi hGradQuasiFermi
   eEparallel hEparallel
   eMobility hMobility
   eVelocity hVelocity
   DonorConcentration AcceptorCncentration
   Doping SpaceCharge
   ConductionBand ValenceBand
   BandGap Affinity
   xMoleFraction
   eTemperature hTemperature
}

Note that electrodes are defined with resistor values that are scaled by the area factor here it is 1000, so the actual source resistance implied is 0.417
DC Solution

- CNormPrint gives the maximum size of the update and the node that it occurs at for each equation solution.

- Fermi specifies Fermi statistics.

- eQuantumPotential is density gradients (a quantum correction particularly for describing the charge in the channel).

- AreaFactor = 1000 is a 1 mm device.

Math {
  CNormPrint
  Extrapolate
  Digits = 5
  NotDamped=1000
  Iterations=25
  NewDiscretization
  ConstRefPot
  ElementEdgeCurrent
  Derivatives
  RelErrcontrol
  NUpperLimit=1e40
  RhsFactor=1e20
  CdensityMin=1e-10
  ErrRef(electron)=1e8
  ErrRef(hole)=1e8
  DirectCurrent
}

Physics {
  Fermi
  eQuantumPotential
  HeteroInterfaces
  AreaFactor = 1000
  Hydro(temperature)
  Recombination( SRH Auger )
}

Describe the Physics

Here a mole fraction of 20% is given

InGaAs has a 30% mole fraction but as it is strictly defined using the software this would be 70% Indium (we have our own internal materials file which has the opposite specification)
DC Solution

Solve {
   Coupled(Iterations=50) { Poisson }
   Coupled(Iterations=50) { Poisson Electron Hole }
   Coupled(Iterations=50) { Poisson eQuantumPotential }
   Coupled(Iterations=50) { Poisson Electron Hole eTemperature eQuantumPotential }

   Quasistationary ( 
      InitialStep=2e-2 Minstep=1e-8 MaxStep=0.20 Increment=1.4 
      Goal { Name="Gate" Voltage=2 } 
   )
   { 
      Coupled { Poisson Electron Hole eTemperature eQuantumPotential } 
      currentplot ( time=(range=(0 1) intervals=40 ) ) 
   }
   Quasistationary ( 
      InitialStep=5e-2 Minstep=1e-8 MaxStep=0.20 Increment=1.4 
      Goal { Name="Drain" Voltage=2.0 } 
   )
   { 
      Coupled { Poisson Electron Hole eTemperature eQuantumPotential } 
      currentplot ( time=(range=(0 1) intervals=5 ) ) 
   }
   Quasistationary ( 
      InitialStep=5e-2 Minstep=1e-8 MaxStep=0.20 Increment=1.4 
      Goal { Name="Drain" Voltage=2.0 } 
   )
   { 
      Coupled { Poisson Electron Hole eTemperature eQuantumPotential } 
      currentplot ( time=(range=(0 1) intervals=5 ) ) 
   }
}

To get initial solution use coupled solutions with additional equations

Current plot gives solutions at predefined points

Sweep the gate, then the drain, then sweep the gate back to get cut off
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Mixed mode allows the user to do circuit simulation with ideal circuit elements and device simulation elements. This can be used for DC, AC, and for transient simulations.

Describe each device and give them a name:
- Then in the system section describe a circuit
- This may be simple or complex

```
Device FET1 {
  Electrode {
    { name="source" voltage=0 Res=200 }
    { name="drain" voltage=0 Res=200 }
    { name="gate" voltage=0 Res=200 }
    { name="sub" voltage=0 Res=200 }
  }
  Physics {
  }
  Plot {
  }
  Math {
  }
  File {
  }
  System {
    FET1 DEV ( drain=dt gate=gt source=st sub=st)
    v v_g(gt 0) {type="dc" dc=0}
    v v_d(dt 0) {type="dc" dc=0}
    v v_s(st 0) {type="dc" dc=0}
  }
```
AC solution

Solve {
   Coupled(Iterations=100) { Poisson }
   Coupled(Iterations=50) { Poisson Electron Hole }
   Coupled(Iterations=50) { Poisson eQuantumPotential }
   Coupled(Iterations=50) { Poisson Electron Hole eTemperature eQuantumPotential }

   Quasistationary {
      InitialStep=1e-2 Minstep=1e-7 MaxStep=0.2 Increment=1.4
      Goal { Parameter=v_g.dc Voltage= 2.0 }
   }
   Coupled { Poisson Electron Hole eTemperature eQuantumPotential }
}

Quasistationary {
   InitialStep=1e-2 Minstep=1e-7 MaxStep=0.2 Increment=1.4
   Goal { Parameter=v_d.dc Voltage= 2 }
}
   Coupled { Poisson Electron Hole eTemperature eQuantumPotential }
}

Quasistationary {
   InitialStep=1e-2 Minstep=1e-7 MaxStep=0.2 Increment=1.4
   Goal { Parameter=v_g.dc Voltage= 0 }
}
   currentplot (time=(range=(0 1) intervals=40 ))
   ACCoupled ( StartFrequency=0.5e9 EndFrequency=20.0e9 NumberOfPoints=39 Linear
   Node(gt dt) Exclude(v_d v_g)
   ACCompute (time=(range=(0 1) intervals=40 ))
   } { Poisson Electron Hole eTemperature eQuantumPotential }
}
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Calibration
What does it mean?

First: Determine every parameter possible from measured data and from the literature
► For the parameter values that cannot be determined determine the reasonable range
  • Calibration
    ▪ Get only the parameters that cannot be directly determined from comparison of simulation to measured data
    ▪ Use only values for these parameters that are within the reasonable range for that value
    ▪ Objective of this procedure is to keep the device simulation physical
    ▪ Can be viewed as a fudge, or it can be viewed as a creative way of measuring that parameter

  • How is calibration different from a model fitting
    ▪ Models may be nonphysical and are fit to a range of measured data
      – As a result the model is only valid in the range of the measured data it was fit to
    ▪ Physical device simulation uses a physical description of the device and mechanisms at grid points
      – A few parameters are set so that this fits a range of data
      – Simulation is predictive because of the basis in physics used beyond the range of the calibration data, this is unlike a model
      – Calibration procedure should not violate the physical description
      – It is important to us a good calibration procedure
Calibration to measured data
FET Procedure

1. Determine barrier height in the simulation by calibrating barrier height to fit measured gate current
2. Set mobilities and contact resistance from measurements, you really want measured mobilities
3. Adjust total charge to get the threshold voltage seen in measurements
4. Set surface trap density/mobility to get sheet resistance seen in measured data
   1. You really want to use measured mobilities,
   2. if you do any adjustment to Rsh is in surface traps or sheet charge, you should have the sheet charge right under the channel if the threshold is right
5. Adjust the saturation velocity to achieve the measured maximum current
6. Add extrinsic inductance determined from small signal AC data
7. When you are done the resistances in each region of the device should add up to the on resistance, this is a useful check and allows you to look for inconsistencies
Calibration to measured data
HBT Procedure

1. Compare gummels, your intrinsic diode parameters from simulation should be good

2. Calibrate beta by emitter and collector resistance at high current and recombination at low current …
   - Important parameter is bandgap narrowing

3. Adjust surface traps to take into account lateral regions

3. Consider impact of bulk traps

4. Differences between two dimensional assumptions and 3 dimensional layout
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Examples: Objectives of TCAD

► Good device physics and a good understanding of device design are required to get a lot out of simulation

► These are some concepts that have been shown to be useful in the past
  • Fets
    ▪ Device doping is chosen by the tradeoff between current and breakdown
    ▪ Focus on device designs that show different trends in this tradeoff
    ▪ Remember FETs are impacted by surface effects, make sure you match the sheet resistance of the device in all regions
  • HBTs
    ▪ Bulk parameters are more important
    ▪ Fitting Gummels and beta curves typically involves some adjustment of recombination parameters including band gap narrowing
    ▪ Surface effects are important near contacts
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Example HBT

- HBT’s are described using similar methods as in other devices
- Vertical grid spacing is typically decreased in junction regions
  - and lateral grid spacing is typically decreased around lateral device discontinuities such as contacts and etches
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Example GaAs MOSFET

The device as a Gadolinium GaAs Oxide layer under the gate, it employs delta doping and a InGaAs Channel.

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs Oxide ( \kappa = 20 )</td>
<td></td>
</tr>
<tr>
<td>2 nm undoped Al(_{45})GaAs</td>
<td></td>
</tr>
<tr>
<td>2 nm undoped GaAs</td>
<td></td>
</tr>
<tr>
<td>10 nm undoped In(_{30})GaAs</td>
<td></td>
</tr>
<tr>
<td>2 nm undoped GaAs</td>
<td></td>
</tr>
<tr>
<td>3 nm undoped Al(_{30})GaAs</td>
<td></td>
</tr>
<tr>
<td>65 nm undoped Al(_{30})GaAs</td>
<td></td>
</tr>
<tr>
<td>0.2 ( \mu )m undoped GaAs</td>
<td></td>
</tr>
<tr>
<td>GaAs Substrate</td>
<td></td>
</tr>
</tbody>
</table>
Example GaAs MOSFET

- Vertical grid must be small in the active region from the surface past the channel
- Gate voltage sweep convergence is impacted by the vertical grid
- Key points are the surface, channel, delta doping, and barrier region
- Lateral gridding is needed at the edge of lateral discontinuities in the structure, such as the gate edges, source and drain edges
- Recesses also create lateral discontinuities
- Drain voltage sweep convergence is impacted by the lateral grid
Simulated and Measured: Id/Vg Characteristics

- The activation of charge is adjusted to about 0.65 (out of 1.0) to get the threshold seen in the measured data
  - Threshold of ~0.25 volts is achieved

- Log(Id)/Vg characteristic shows the sub-threshold swing (s) of 100 [mv/dec]
Simulated vs Measured \( I_d/V_d \) Characteristic

- Set saturation velocity to 1.3e7 cm/sec
  - This is not completely physical
- Set the effective contact resistance to achieve the same on resistance observed in the device
  - This usually has to do with access resistance which is not typically accurately measured
  - In this case the access resistance used in the simulation was \(~0.6\text{ ohm mm}\)
Comparison to measured data

Comparison of some of the device characteristics to measured data

Differences in $R_c$ suggest
- The meas $R_c$ is bad, or
- The sim has lower $R_{ch}$

<table>
<thead>
<tr>
<th>par</th>
<th>Simulation</th>
<th>Measured</th>
<th>Error</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{th}$</td>
<td>0.254</td>
<td>0.25-0.27</td>
<td>on</td>
<td>volts</td>
</tr>
<tr>
<td>$R_{on}$</td>
<td>2.23</td>
<td>2.25</td>
<td>0.9%</td>
<td>ohm mm</td>
</tr>
<tr>
<td>$S$</td>
<td>100</td>
<td>106</td>
<td>6%</td>
<td>mv/dec</td>
</tr>
<tr>
<td>$I_{dss}$</td>
<td>427</td>
<td>435-421</td>
<td>&gt;2%</td>
<td>mA</td>
</tr>
<tr>
<td>$R_{sh}$</td>
<td>461</td>
<td>449</td>
<td>2.6%</td>
<td>mA</td>
</tr>
<tr>
<td>$R_c$</td>
<td>0.617</td>
<td>0.417</td>
<td>47%</td>
<td>ohm mm</td>
</tr>
</tbody>
</table>

Check

$R_{on} = 2*R_c + 0.85*2*R_{sh} + L_g*R_{ch} \approx 2.25\ \Omega$
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AC characteristics

- The “intrinsic” device in the inner box is simulated using TCAD but this is not exactly what is built in the laboratory.
- The external box contains the extrinsics seen there.
- In order to assess the AC characteristics the extrinsic parasitics must be considered/added.
- The output of simulator is conductance and acceptance at the ports, which can be converted to y, z or s.
- To add extrinsics convert TCAD results to z parameters and add

\[
\begin{bmatrix}
R_g + L_g \cdot \omega \cdot i + (R_s + L_s \cdot \omega \cdot i) \\
(R_s + L_s \cdot \omega \cdot i) \\
R_d + L_d \cdot \omega \cdot i + (R_s + L_s \cdot \omega \cdot i)
\end{bmatrix}
\]

- Then convert back to y or s parameters.
S parameters that result, both intrinsic and extrinsic S parameters are shown.

\[
\begin{align*}
G + iA & \rightarrow Z & \rightarrow S_{\text{intrinsic}} \\
Z + Z_e & \rightarrow S_{\text{extrinsic}}
\end{align*}
\]
Small Signal Gain

Add gate resistance
Gate inductance
Load inductance

Impact of these parasitics is, Fmax is decreased from from ~200 to 20 GHz

Source inductance …
You must have a good handle on parasitics to get the right answer

► Impact of Source Inductance is to significantly reduce the corner frequency which results in lower gain at high frequency

In some cases the source inductance is not well known but can be set to achieve the gain observed
You must have a good handle on parasitics to get the right answer

► This is the impact of the gate resistance,
► TCAD simulations typically don’t include the gate resistance.
► Increases in gate resistance also impact the gain curve and the location of the corner frequency.
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PHEMT Switch Evaluation of Harmonics

- SPDT Switch implemented with PHEMT multi gate switches

![Single Pole Double Throw Switch Diagram]

![PHEMT TCAD Calibration to Measured Data Graph]

- DC I/V
- S param
Single Pole Double Throw Switch Simulation

System {
  *-----------------------------------------------------------------------*
  HEMT phemt (Source=s Drain=d Gate1=g1 Gate2=g2 Gate3=g3)
  Plot "switch" (time() v(s) v(d) v(n2) i(s d) i(s n2))
  Vsource_pset vs (vs 0) \{ sine = (0 1.25892541179417 1e9 0 0) \}
  Resistor_pset Rin (vs s) \{ resistance = 50 \}
  Resistor_pset RD (s d) \{ resistance = 16000 \}
  Vsource_pset vc (vc 0) \{ dc = 0 \}
  Resistor_pset Ron (s n2) \{ resistance = 2.35 \}
  Resistor_pset RL_ (n2 0) \{ resistance = 50 \}
  Resistor_pset RL (d 0) \{ resistance = 50 \}
  Resistor_pset RG1 (g1 vc) \{ resistance = 16000 \}
  Resistor_pset RG2 (g2 vc) \{ resistance = 16000 \}
  Resistor_pset RG3 (g3 vc) \{ resistance = 16000 \}
  *-----------------------------------------------------------------------*
}

* Switch circuit
*-----------------------------------------------------------------------*

More complex mixed mode simulations can be done including ones with multiple active devices and ideal passive components, here a single pole double throw circuit is described
Switch Simulation

In this case we are doing a single pole double throw simulation with a switch composed of two devices.
Transient Simulations

► This is the resulting device simulation showing the transient solution of the off state device.
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There are three ways to do large signal simulations using TCAD

1. Use mixed mode to simulate transient response of RF circuits
   Simulations are long and difficult, not well integrated with designer problems

2. Use integrated harmonic balance algorithm
   Not operable for practical problems, long simulations, not well integrated with designs

3. Extract a model based on TCAD
   Limits to what the model is capable, well integrated with designer
Heterostructure process and device simulation can be done using basic methods. Key mechanisms necessary for FETs and Bipolars are available in commercial vendor packages. Methods exist that make it possible to integrate known material data and calibration to measured data. These methods enable TCAD simulations for DC, small signal AC, and large signal prediction.
References

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Kalna, K., et al. (2007). “Monte Carlo Simulations of High-Performance Implant Free In0.3Ga0.7As Nano-MOSFETs for Low-Power CMOS Applications.” IEEE Transactions on Nanotechnology 6(1).