Alternate Backside Thinning of GaAs-Based Devices

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ABSTRACT

A backside dry-etching process has been developed to completely remove the GaAs substrate and expose the device-processed epilayers on it. The process is uniform, reproducible, and preserves the properties and yield of the processed devices. Infrared images produced by focal plane arrays (FPAs) thinned using this alternate backside process, directly and vividly demonstrate the quality of this process.

INTRODUCTION

The conventional method of backside substrate removal is chemical-mechanical polishing [1,2,3]. This method suffers from poor control of the substrate removal which can lead to erosion and damage (lapping-induced stress) of sensitive epilayers (such as GaAs/AlGaAs quantum wells) grown on the substrate. Chemical-mechanical polishing requires the presence of relatively thick (~ 1000 nm) AlGaAs etch-stop layers between active device layers and substrate. Such thick layers involve longer MBE growth times, result in proportionately higher growth-defect-densities and increase cost. These growth defects are partially responsible for reducing pixel operability in Quantum Well Infrared Photodetector (QWIP) Focal Plane Arrays (FPAs).

There are numerous papers in the literature that report on low-damage selective dry etching of GaAs/AlGaAs-based device structures using BCl3/SF6 and SiCl4/SF6 [4,5,6,7]. However, limited information is available on the backside thinning of GaAs-based devices utilizing plasma etching.

This alternate substrate-removal process allows for a much thinner (< 50 nm) AlGaAs etch-stop layer with lower Al concentration (30%). These features lower growth defect density and improve device yield. Using optimized etch parameters, an extremely uniform two-step etch process was developed yielding GaAs etch rates up to 3 μm/min with minimal device damage, and GaAs-to-AlGaAs selectivity > 1000.

EXPERIMENTAL

An Oxford Plasma Technology µP RIE [170 mm water-cooled (30°C) quartz-covered aluminum lower electrode, 300 watt 13.56 MHz ENI RF generator] was used to develop a highly-selective SF6/SiCl4 etch process for the backside thinning of GaAs substrates, stopping on an underlying AlGaAs layer. A statistically-designed experiment was performed to optimize the process with regard to the backside GaAs etch rate and backside GaAs surface morphology. This experiment was selected in order to optimize the response variables, indicate major trends, and determine the direction for future experimentation. Main and interaction effects were calculated and plotted.

Samples used to study GaAs backside etch rate and surface morphology consisted of 3-inch GaAs substrates with 3000 nm of patterned positive resist. Surface morphology was determined by rating scanning electron microscopy (SEM) photographs after the samples were etched. For the purpose of comparison, all samples were etched for 15 minutes. Etch rate was determined from thickness measurements (after resist removal) using a Tencor alfa-step 200 film thickness system.

Samples used to study selectivity consisted of 1.5 cm x 1.5 cm clear-field-resist-patterned 1000 nm-thick n-type MBE-grown AlxGa1-xAs (0.10<x<0.50). For the purpose of comparison, all samples were etched for 10 minutes. Selectivity to AlxGa1-xAs (0.10<x<0.50) was determined by dividing the etch rate of the GaAs by the etch rate of the AlGaAs.

Samples used to study damage consisted of 1000 nm-thick Al0.30Ga0.70As grown by MBE and n-doped with Si to a concentration of 1x1018 cm-3. Plasma exposure times were chosen to simulate the plasma exposure that the AlGaAs surface would see during the over etch step. Damage test exposure times were 300 seconds. Damage is defined as the change in sheet carrier concentration [ΔNs = Ns(control sample) - Ns(damage test sample)], obtained by Polaron measurements.

EXPERIMENTAL RESULTS AND OBSERVATIONS

A 23 factorial designed experiment was performed to study the potential for possible interaction between the control parameters and optimize the process with regard to the GaAs etch rate and GaAs surface morphology. Table 1 highlights the run conditions for the experiment. Several reports [5,6] have shown that GaAs to AlGaAs selectivity peaks with a 2:1 SiCl4:SF6 ratio. Therefore, to maximize selectivity the SiCl4:SF6 ratio was held constant at 2:1 for the duration of the experiments. Electrode temperature was fixed at 30°C.

TABLE 1
Factorial Designed Experiment: High and low settings for control parameters as well as the fixed settings for gas ratio and electrode temperature.

<table>
<thead>
<tr>
<th>Control Parameters</th>
<th>Low Setting</th>
<th>High Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF power (watts)</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>Chamber Pressure (mTorr)</td>
<td>30</td>
<td>70</td>
</tr>
<tr>
<td>Total Flow (sccm)</td>
<td>20</td>
<td>40</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Control Parameters</th>
<th>Fixed Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gas Ratio SiCl4:SF6</td>
<td>2:1</td>
</tr>
<tr>
<td>Electrode Temperature</td>
<td>30 °C</td>
</tr>
</tbody>
</table>

Results of the study showed an interaction between RF power and chamber pressure with regard to backside GaAs etch rate. Figure 1 indicates that at 70 mTorr the etch rate increases with increasing RF power (chemical/isotropic etch characteristics). However, at 30 mTorr the etch rate decreases with increasing RF power (physical/anisotropic etch characteristics).

Surface morphology of the GaAs improved with decreasing total flow (increasing ion to neutral flux ratio) and decreasing RF power (lower ion energy).

Additional experiments were performed to further investigate selectivity of GaAs to Al<sub>x</sub>Ga<sub>1-x</sub>As (0.10<x<0.50). With optimized parameters (70 mTorr, 20 sccm total flow, 2:1 SiCl<sub>4</sub>:SF<sub>6</sub>, and 30°C electrode temperature), 1.5 cm x 1.5 cm Al<sub>x</sub>Ga<sub>1-x</sub>As 1000 nm-thick n-type MBE-grown samples were etched at different pressures utilizing the optimized parameters (75 watts, 20 sccm total flow, 2:1 SiCl<sub>4</sub>:SF<sub>6</sub>, and 30°C electrode temperature). A plot of Al<sub>x</sub>Ga<sub>1-x</sub>As etch rate vs. chamber pressure (Fig. 4) shows that the Al<sub>x</sub>Ga<sub>1-x</sub>As etch rate increased with decreasing pressure (increasing Bias -Vdc).

The results, presented in Fig. 5 show that selectivity increases with both increasing Al concentration and RF power (ion energy). Selectivity reaches infinity with 50%
Al and RF powers less than 125 watts. This is due to the fact that the AlGaAs etch rate (after 10 minutes of etch time) drops to 0 nm/min below 125 watts of RF power.

To investigate plasma damage, n-type AlGaAs samples were exposed to the optimized SF/SiCl$_4$ plasma (70 mTorr, 20 sccm total flow, 2:1 SiCl$_4$:SF$_6$, and 30°C electrode temperature) with varying RF powers. Damage exposure times were 300 seconds (time allowed to completely remove the GaAs substrate). Polaron measurements were used to obtain the change in sheet carrier concentration (ΔNs). The results presented in Fig. 6 show that at RF powers below 75 watts low levels of damage can be obtained. Polaron etch profiles indicate that the plasma damage is localized at the surface of the AlGaAs layer. At 75 watts, 70 mTorr, 20 sccm total flow, 2:1 SiCl$_4$:SF$_6$, and 30°C electrode temperature (300 second over etch), damage (Ns) occurred only ~ 8 nm into the surface of the AlGaAs layer. Based on the above results it appears that a thin (10 nm to 50 nm) 30%-Al AlGaAs etch stop layer is required between active device layers and the GaAs substrate. This thin stop layer is sufficient to eliminate any backside etch damage to the active device layers.

Secondary Ion Mass Spectroscopy analysis of over etched samples showed the formation of the typical nonvolatile AlF$_3$ barrier layer that has been extensively studied in the past.

In order to maximize the etch rate of the GaAs, minimize the damage to the active device layers, and sustain the high GaAs to AlGaAs selectivity, a two-step etch process was implemented. Step 1 (70 mTorr, 100 watts, 20 sccm total flow, 2:1 SiCl$_4$:SF$_6$, and 30°C electrode temperature) is necessary to initiate the etching of the chemical-mechanical polished surface. Step 2 (70 mTorr, 75 watts, 20 sccm total flow, 2:1 SiCl$_4$:SF$_6$, and 30°C electrode temperature) sustains the high etch rate as well as provides low damage and high selectivity.

FIG. 7: A typical smooth etch surface (left) along with the pre-etch (chemical-mechanical polished) rough surface (right) that was masked during the selective etch.

FIG. 8: FPA substrate removal time and pre-etch sample thickness for a number of FPAs.

FIG. 6: The change in sheet carrier concentration (ΔNs) versus RF Power. RF power was varied between 50 and 125 watts. Damage test samples were exposed to the plasma for 300 seconds.

DEVICE RESULTS

In order to confirm the experimental results, the alternative optimized etch process was tested on several QWIP detectors (Al$_{0.50}$Ga$_{0.50}$As stop layer) hybridized to a Si ROIC (Read Out Integrated Circuit). The SEM photograph (Fig. 7) shows a typical smooth etch surface along with the pre-etch (chemical-mechanical polished) rough surface that was masked during the selective etch.
This process is now used in the substrate removal of QWIP detectors hybridized to Si ROIC chips, where it improves photoreponse, eliminates pixel-pixel optical crosstalk, and thermal mismatch between detector and ROIC. Figure 8 shows sample thickness and clear time for processed QWIP FPAs (Fig. 9). Pixel operability in excess of 99.6% is now routinely obtained (Fig. 10) in FPAs with formats as large as 640x480. The technique’s success in producing a smooth and uniform surface (following substrate removal) over a large chip area (typically 16 mm x 12 mm) is directly evident in the high quality of the infrared imaging the FPAs demonstrate (Fig. 11). A typical noise-equivalent temperature difference (NETD) of ~ 20 mK is obtained in the FPAs. The NETD includes both temporal and spatial noise. Spatial NETD is strongly affected by the quality of the backside thinning and its uniformity. FPA imaging probably represents the most sensitive gauge of the quality of the thinning technique. That a NETD value of 20 mK is routinely obtained is a measure of the technique’s quality, uniformity, and reproducibility.

Fig. 9: Cross-section of QWIP FPA bump-bonded to a ROIC/Fanout. The photosensitive QWIP layers are sandwiched between doped contact layers. A metallized grating etched into the top contact couples light incident from the bottom. The etch stop helps in substrate removal; it is removed prior to packaging.

Fig. 10: Pixel operability in the last 34 thinned 640x480 QWIP FPAs. An average operability of 99.56% is obtained. Almost all the dead pixels are randomly scattered, lending themselves to easy ‘image-correction’.

CONCLUSION

Using optimized etch parameters presented in this paper, an extremely uniform two-step etch process was developed yielding GaAs etch rates around 3 µm/min with minimal device damage, and GaAs-to-AlGaAs selectivity near infinity. The technique is now routinely used for substrate removal in high-performing QWIP focal plane arrays.

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