Cost - Effective Yield Enhancement in 6-inch Gallium Arsenide Wafer Manufacturing

P. Bohlinger 1, Y. Z. Wang 1, T. McGuine 2 and C. Nielsen 2

1 Anadigics, Warren, NJ 07059, USA
Telephone: (908) 668-5000, e-mail: pbohlinger@anadigics.com
2 August Technology, Bloomington, MN 55435, USA

Abstract

In this paper, we reported a cost effective yield enhancement methodology in our 6-inch Gallium Arsenide wafer fab using the August NSX system and in-house developed defect correlation program. An automated defect detection and analysis system has been developed to monitor process and defect excursions at the critical process levels. The inspection results are correlated to die sort yield and parametric results to foster continuous improvement. Several successful yield improvements have been achieved in our wafer fab with the implementation of the yield enhancement methodology.

Introduction

Increasing competition within the telecommunication industry is forcing manufacturers to consider and implement yield enhancement in III-V fabrication operations. Controlling defects across all of the critical processes is perceived as being "non-value add" metrology operation, and results in faster cycle time and accelerated production ramp to yield entitlement [1]. However, there is no formal methodology to measure defects and to control the critical processes at in-line patterned wafer inspection for most III-V fabrication operations. This greatly affects yield and technology development because manual inspection results in variable defect capture rates that depend on the ability and experiences of the inspection operators [2]. Data from manual inspections are difficult to archive or correlate with yield and parametric results. It is also hard to drive yield improvement from manual inspection results. An automated in-line patterned wafer inspection system is a key to yield improvement [1,2]. The challenge for this is to control the inspection costs including system cost, direct and indirect labor, training and service.

In Anadigics' 6-inch Gallium Arsenide (GaAs) wafer fab, August NSX automated inspection equipment is employed to establish a reliable, low-cost and high throughput in-line patterned wafer inspection and analysis system. It is used to run full wafer inspection, and to monitor defects at the critical process steps for Metal-Semiconductor Field-Effect Transistor (MESFET), Heterojunction Bipolar Transistor (HBT) and pseudomorphic High Electron Mobility Transistor (pHEMT) products and to correlate the defects to die sort yield and parametric results at probe testing, hence improve the yield by reducing the critical defect density.

August NSX System

August NSX series is designed for micro defect inspection of the active die area of processed wafers. The system consists of defect inspection station and wafer handling station, which are controlled by software from wafer handling to defect detection. It runs wafer inspection automatically after an inspection model and recipe setup are created and stored. After inspection is completed an inspection report and defect map for each wafer are generated. Inspection data and images can be displayed, stored, printed or exported onto other system networks. Based on quality optics, computer-controlled illumination and auto focus, the NSX system is able to detect micro defects down to sub-micron. Within the pixel resolution of 0.6 \( \mu \text{m} \), the total repeatability and reproducibility is ~20% [3], which satisfies the current applications in our GaAs wafer manufacturing.

The large-variation in die sizes of our GaAs products makes defect detection and analysis more challenging. The NSX is able to scan down large active area that covers several small dies, and to identify defects on the small individual die including partial die at the wafer edge based on user definable inspection recipe. One of the NSX attractive advantages is the control of inspection costs. The NSX is cost-effective from the system itself, training, service and spare parts.

Defect Monitor and Excursion Control

An NSX-90 system has been introduced into our 6-inch GaAs wafer fab to perform in-line patterned wafer inspection. An automatic defect detection and analysis system has been developed to monitor process and defect excursions on MESFET products at four critical processes in our wafer fab. The inspection system is optimized to capture minimum defects down to size of 1.5 \( \mu \text{m} \) at the active die area. The well-established defect baseline at each critical process level and the inspection-sampling plan are able to capture most of the process-related defect excursions – amount of defective dies exceeds the defect baseline [1]. In order to minimize the resulting yield loss from a defect excursion, the excursion must be quickly detected, and the necessary corrective action must be taken. The defect
excursion is fed back to wafer fab to improve and enhance the yield. Figure 1 shows defect excursion frequencies and die yield impact at the four critical process levels A, B, C and D during the production ramp in our 6-inch wafer fab. Level D has the highest excursion frequency and also has the highest die yield impact in these four inspection levels. The higher the excursion frequency and the die yield impact, the more critical the process. The defective die percentage per wafer versus defect type for the defect excursion is shown in Figure 2, which indicates defect types of F1, F3, F12 and F9 are the major defect types in the excursions at the four levels. This figure also shows the average defective die percentage rolling four weeks. The same four types of defects are dominant in the defect excursions that means these types of defects appeared consistently during the production ramp up. Figure 3 shows the defect distribution at the four critical levels. F1 is the major defect type at Level D.

The detected defect types are isolated to determine root causes by correlating to the resources. Yield teams are formed within specific areas to determine root causes and to perform continuous improvements. When the root causes are corrected, the yield limiting defects sharply decrease. Figure 4, for instance, shows the difference of defective die percentage caused by F3 type on metallization at level A before and after the root cause was corrected. The root cause for this type of defects was the process prior to metallization. Although the type of defects was observed in manual inspection, no statistical data was available to correlate with the yield loss, it was considered as low level and ignored. The NSX inspection detected the defects across wafer. It is clear as indicated in Figure 4 that the defective die percentage is sharply decreased after two actions were taken to improve the yield.

With implementing NSX system, we are able to detect the special types of defects that are frequently missed in manual inspection. Mask defect is one of the defect types that are often missed by operators in manual inspection because of the smaller defect size and the limited inspection area across wafer. However, this type of defect is easily detected by NSX system since it has strong repeatable features from field to field on the defect map. When the defect location is identified within die from defect images, the defects can be quickly corrected to reduce the effects on the incoming lots.
The difference of defective die percentage caused by F3 defect type on metallization at level A before and after the root cause was corrected.

**THE CORRELATION OF IN-LINE INSPECTION TO PROBE TESTING RESULTS**

It is important to establish database and analysis system to correlate the in-line patterned wafer inspection results to diesort yield and parametric results at probe testing. In-house software “Yield Analysis System – Defect Correlation” has been developed to correlate the patterned wafer defect maps to the probe testing maps. The system highlights any correlation between NSX defect inspection and die failure at probe testing. It works by overlaying the wafer maps from NSX inspection and diesort probe testing via a “reference die wizard” by selecting lot and wafer numbers. In this way, the correlation of yield loss at probe to manufacturing defects is easily identified. As shown in Figure 5, the system not only displays the wafer defect map, probing map and their overlay, it also displays Pareto charts showing the breakdown of defects by categories. The system is also able to compare defect maps at two more NSX inspection levels from the same wafer and displays their overlay. One of the important functions of the system is its ability to export the wafer maps, charts and raw data to Microsoft Excel for further analysis.

Figure 6 shows the diesort yield loss and the defect overlay at different probing parameter bins on one wafer. As shown in Figure 6 Bins 2 and 1 are the major diesort failures on the wafer. Both bins have the overlay with process defects, which indicates that some diesort yield loss for both of bins may be due to the process defects. Parametric failures on Bin 3 and Bin 4 have no overlay with process defects.

Figure 7 breaks down the NSX defects by categories for the wafer shown in Figure 6 and shows the Bin 1 and Bin 2 overlays in the defect categories. It is clear that on this special wafer the type F2 defects overlay both of Bin 1 and Bin 2 yield loss, and some defects of type F3 overly Bin 1 and Bin 2 yield loss, too. However, the major defect type F1 on this wafer basically shows no impact on diesort yield loss. This indicates that defect types of F2 and F3 may be the killer defects. The correlation of diesort yield loss to process defects strongly depend on the defect type, it also depends on the defect density and location in the die active area, as well as on the device design and yield sensitivity. This yield analysis system provides us a quick and easy off-line analysis on the correlation of NSX defects to diesort yield.
loss. More detail analysis can be done by viewing defect list and defect density chart.

Figure 7. The NSX defects by categories for the wafer shown in Figure 6.

A good example of the correlation of diesort yield loss to the NSX defects is the ring pattern yield loss at probe testing as shown in Figure 8(a). The yield loss due to the current failure has been occurred on some products, however it couldn’t be correlated with an operation until we observed the similar ring pattern defects on NSX inspection as shown in Figure 8(b). From NSX inspection we understand that the defects are generated between Level A and Level B. The experiments on creating the defects at the suspected resource showed the same defect pattern. The analysis of root cause and defect elimination are in progress.

SUMMARY

An automated defect detection and analysis methodology using NSX system has been developed to monitor in-line patterned wafer process and defect excursions in our 6-inch GaAs wafer fab. The defect results are fed back to wafer fab for yield improvement, which has lead to several continuous improvement actions resulted in the reduction in defects. An in-house developed program is used to correlate the in-line patterned wafer inspection results to diesort yield and parametric results. It has resulted in some great progress in reducing diesort yield loss. With yield improvement, the excursion rates and yield loss are decreased and thus, the cost is reduced. We are on a quest to create “the perfect wafer” in our 6-inch GaAs wafer fab.

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REFERENCE